

Compal Confidential

HBL51 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M

2005-11-03

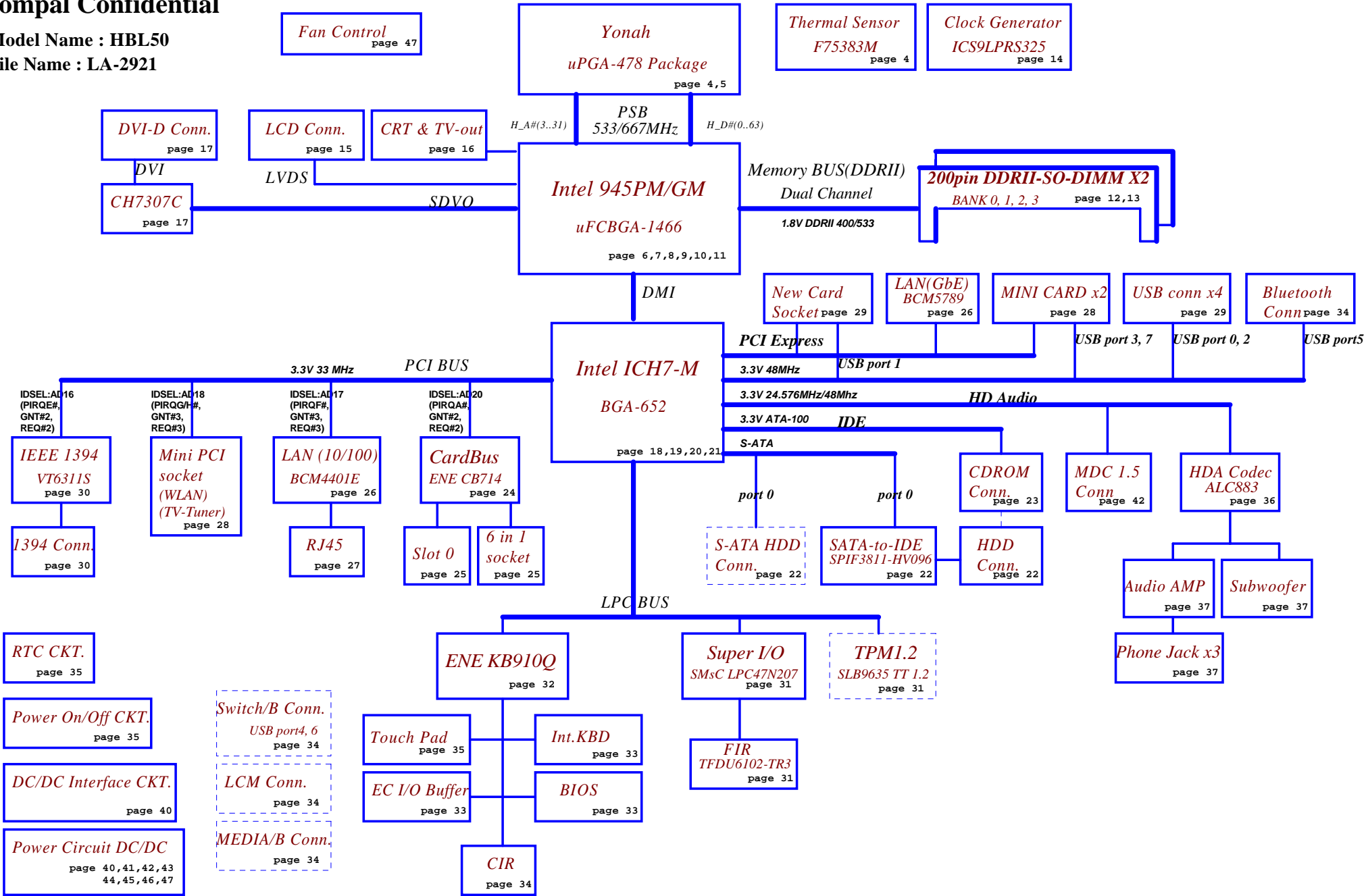
REV: 0.2

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				Cover Page		
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Model Name : HBL50

File Name : LA-2921



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				Block Diagrams	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

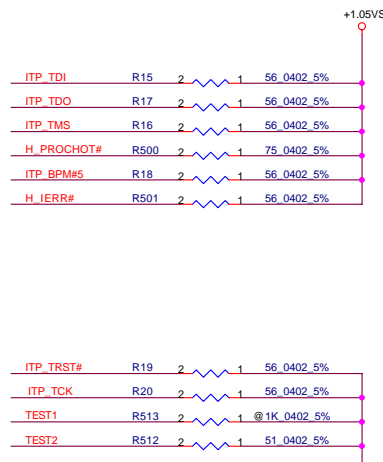
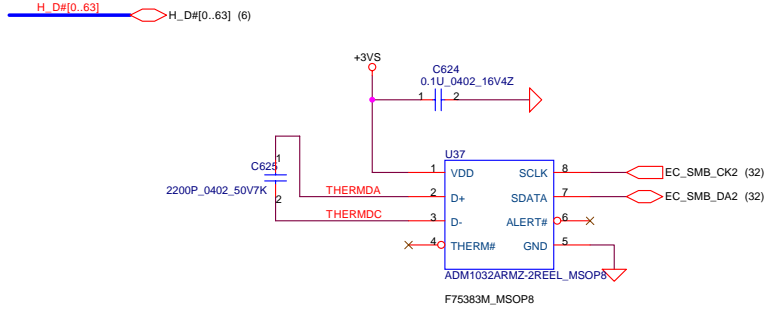
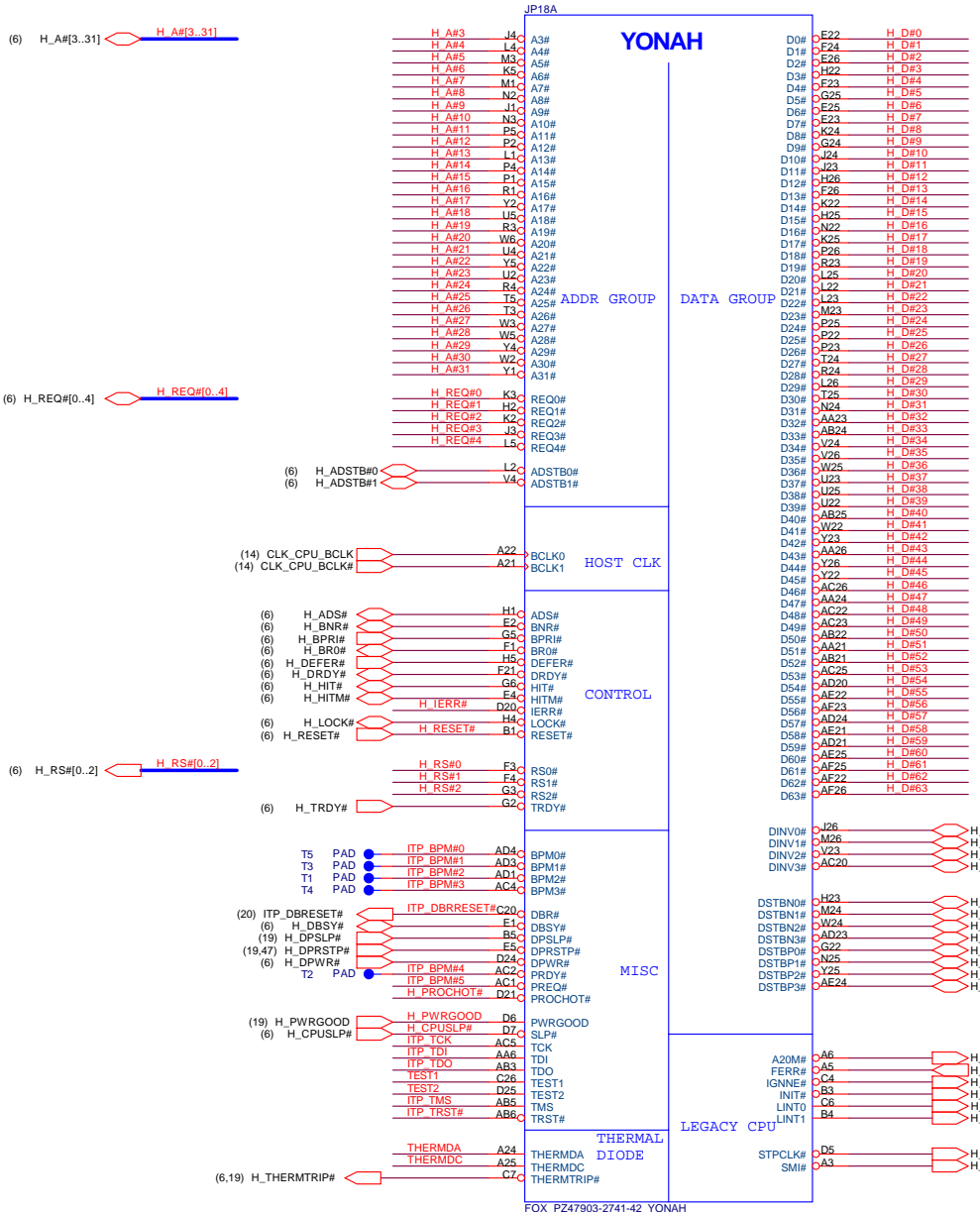
BTO Option Table

BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@

SKU ID Table

SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	

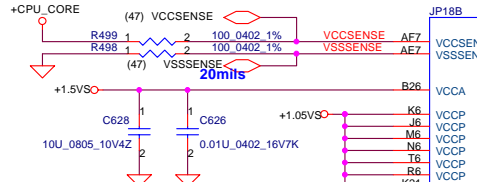
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				Notes List
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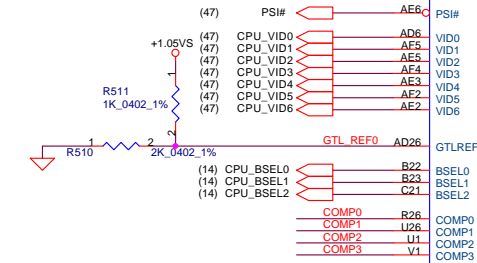
Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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				Yonah (1/2)	
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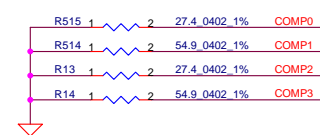
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.



Layout Note:
Place C14 near Pin B26



BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166



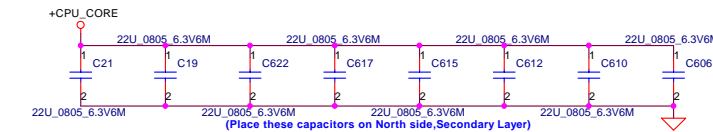
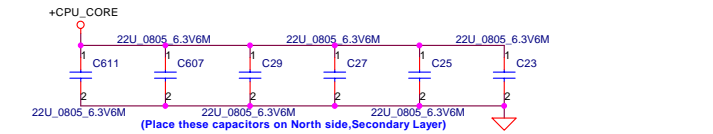
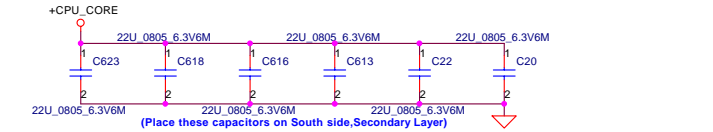
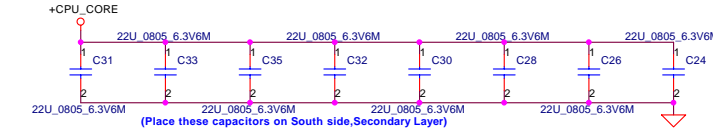
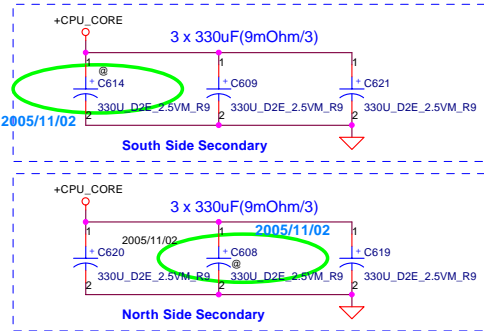
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)
COMP1, COMP3 layout : Space 25mils (55ohms)

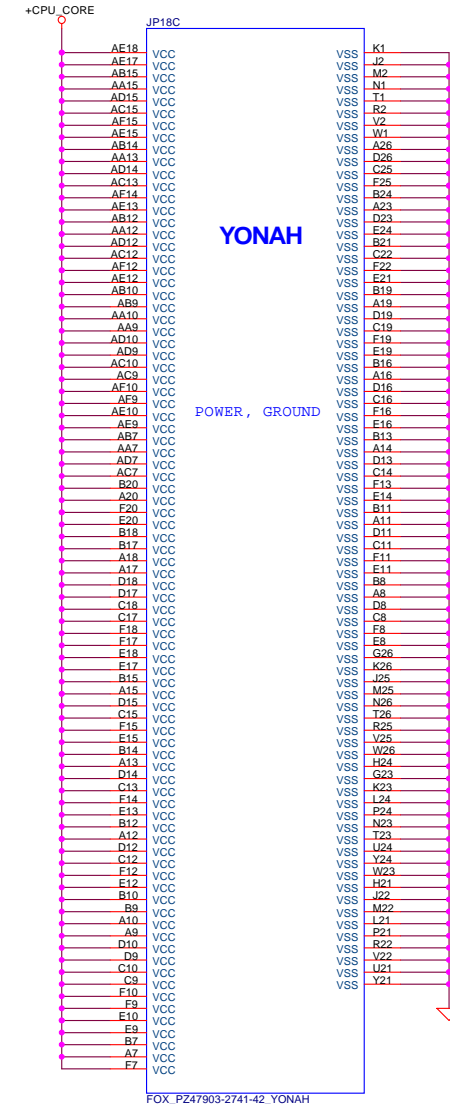
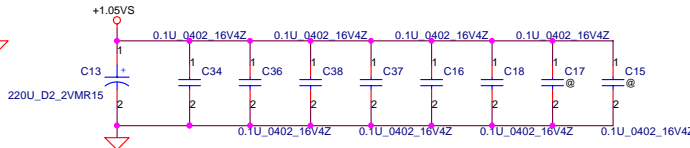
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

FOX_PZ47903-2741-42_YONAH



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32

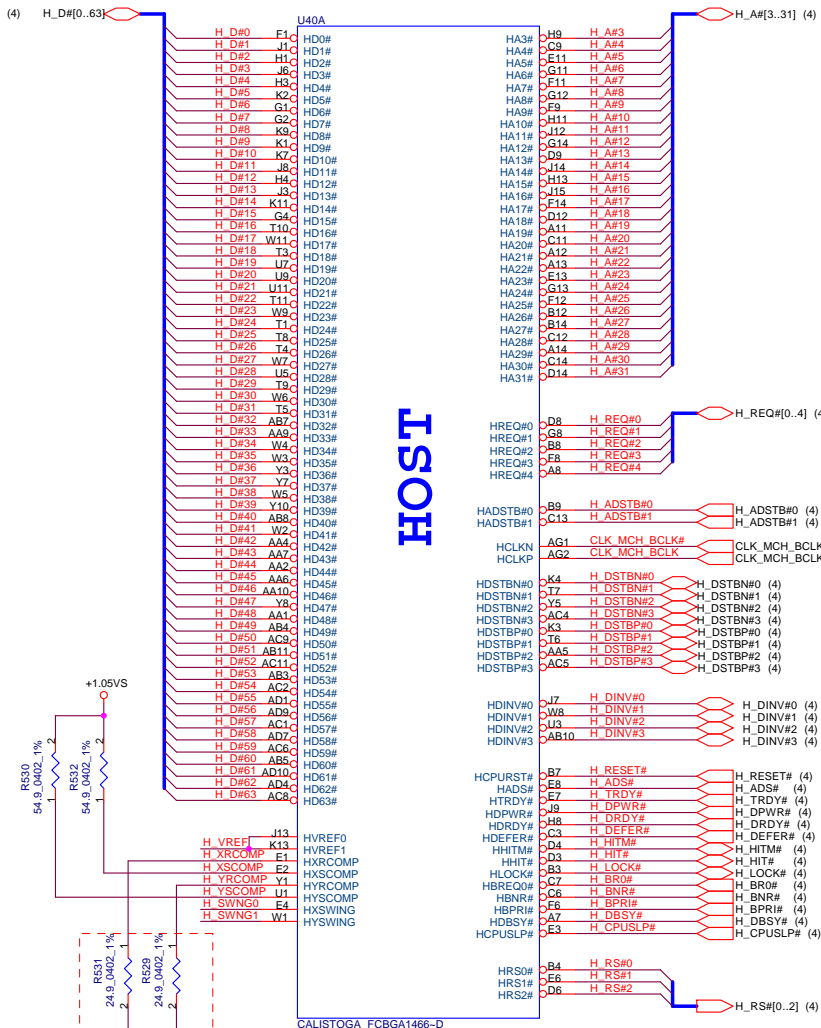


YONAH

POWER, GROUND

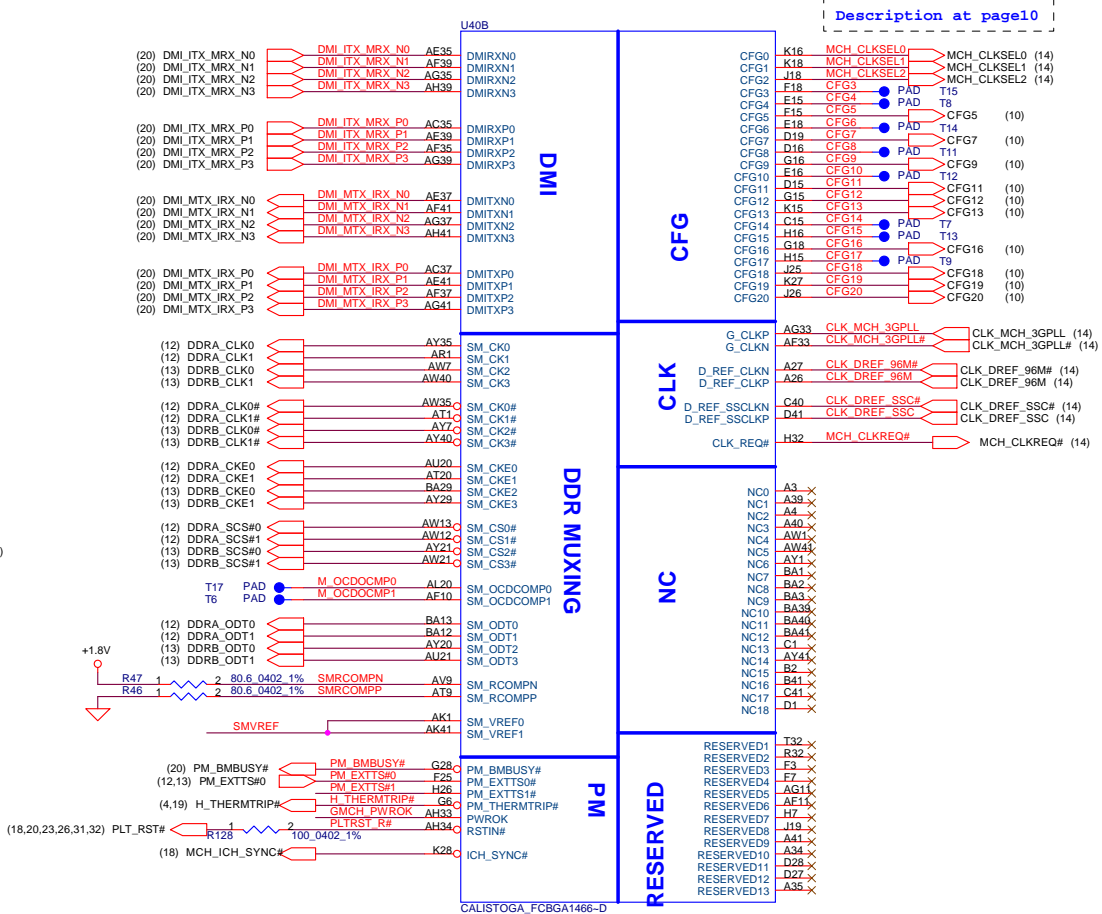
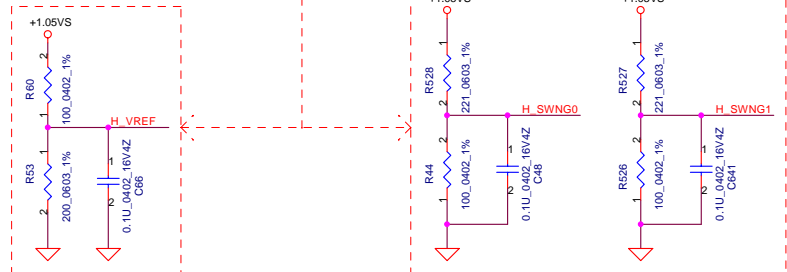
FOX_PZ47903-2741-42_YONAH

945GM(A-1) (QJ15) [ES2]: SA000005970
 945GM(A-2) (QK44) [ES3]: SA000005980
 945PM(A-2) (QK46) [ES3]: SA00000UV10



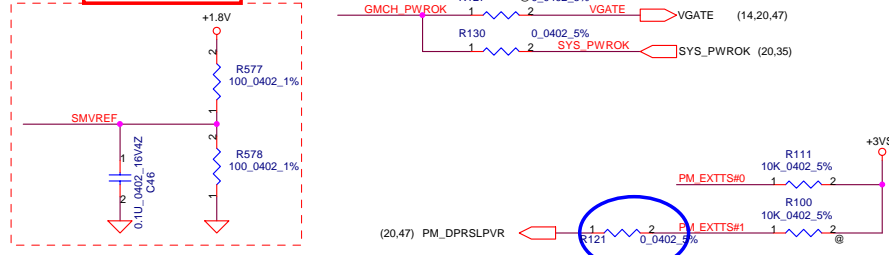
HOST

Layout Note:
 H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.

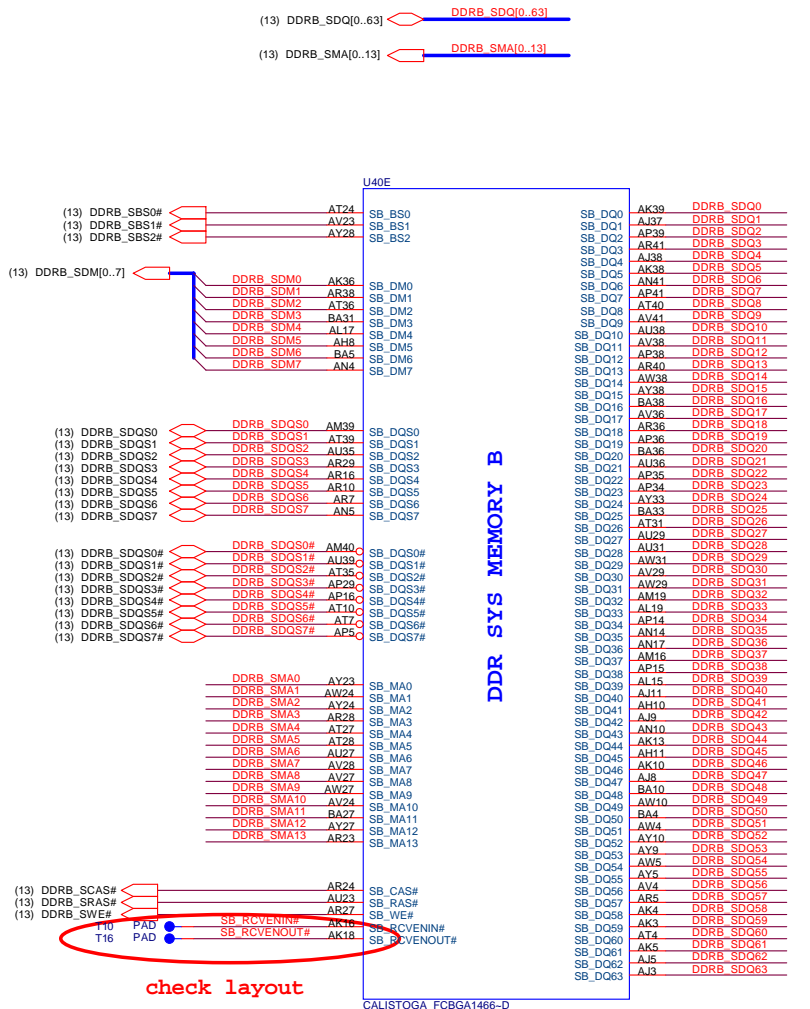
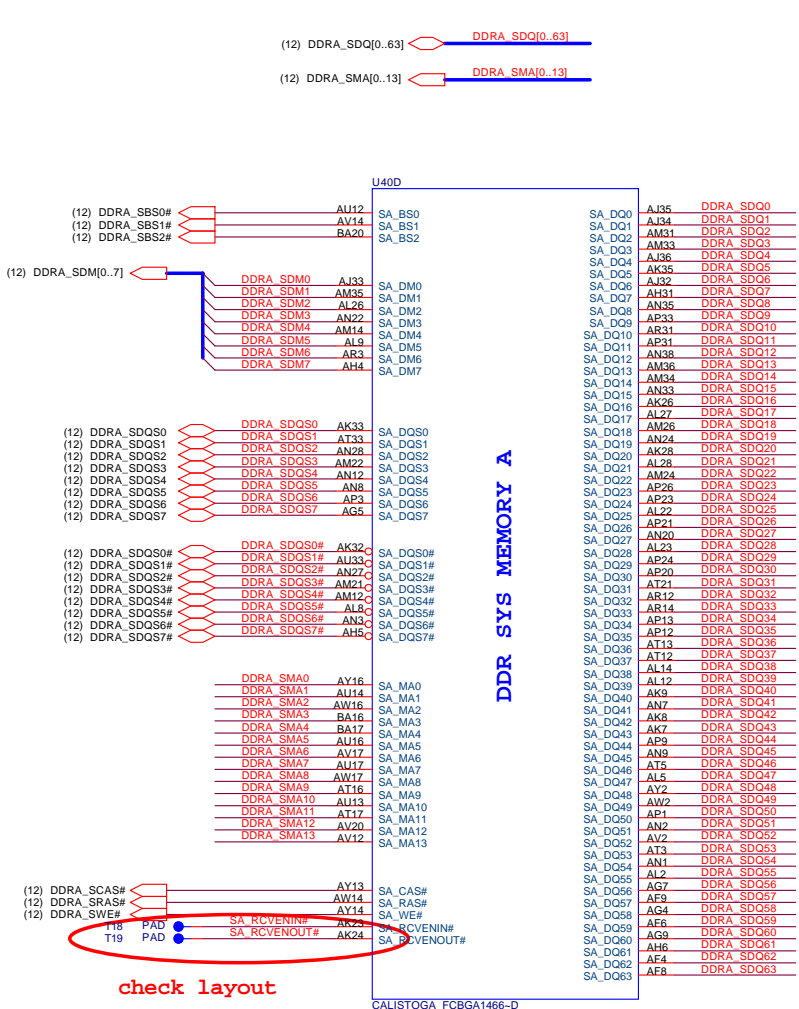


Description at page 10

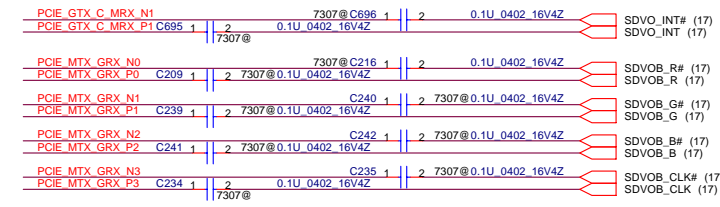
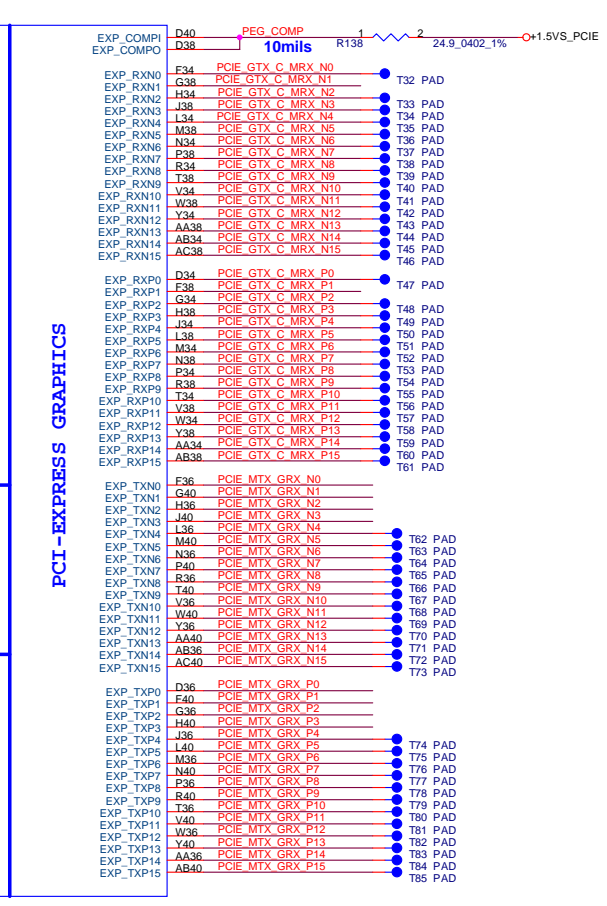
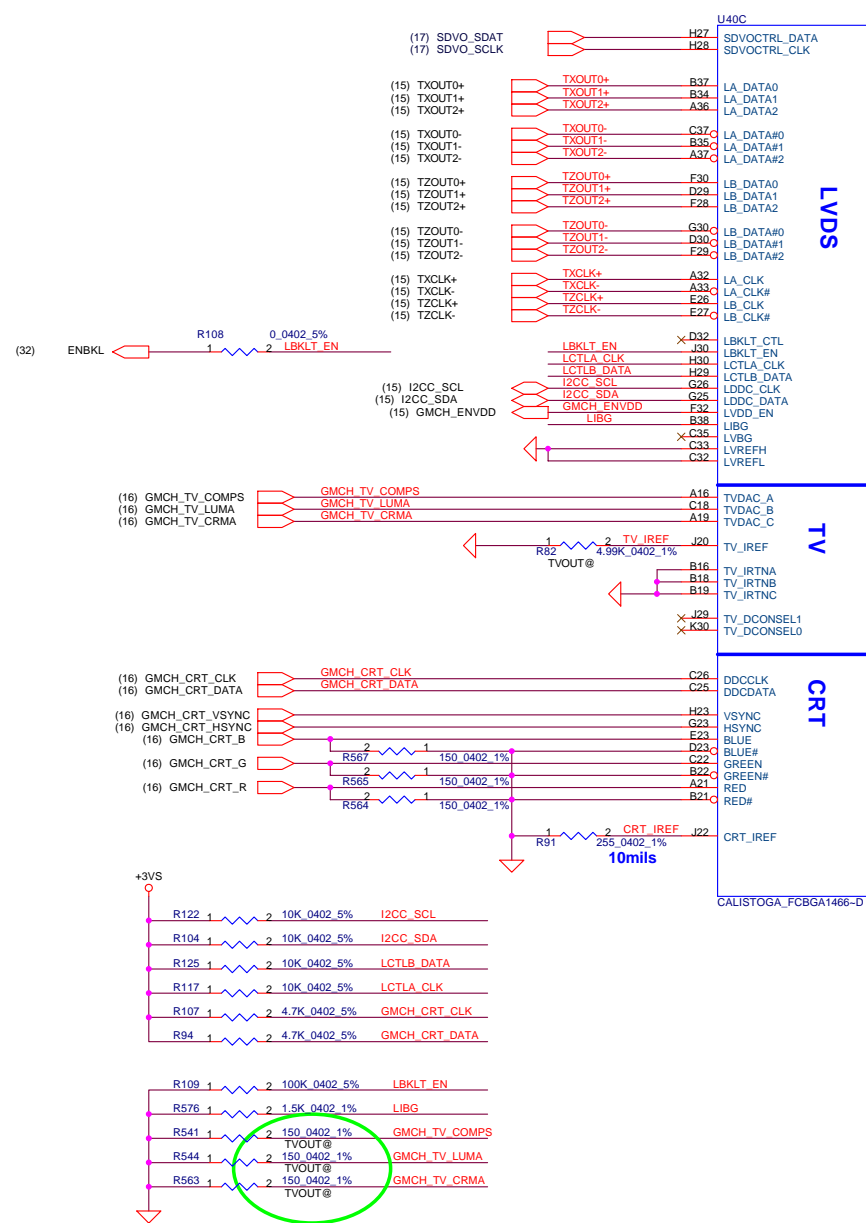
Layout Note:
 SMVREF trace width and spacing is 20/20.



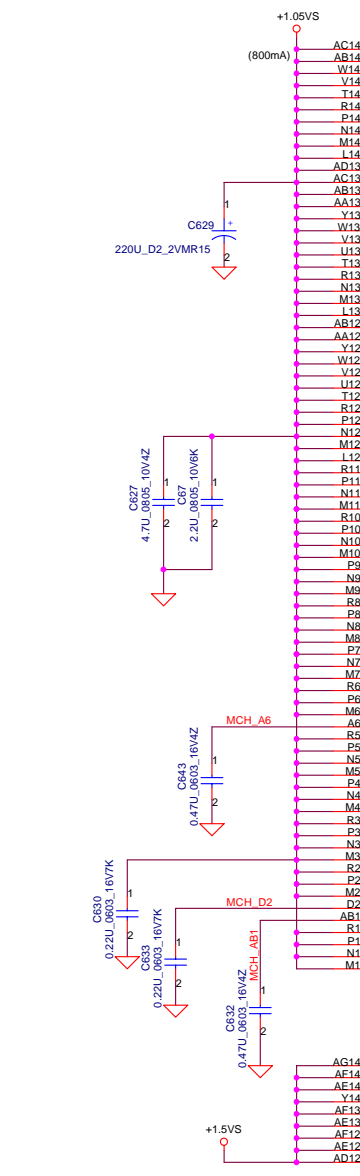
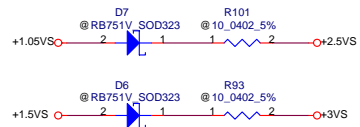
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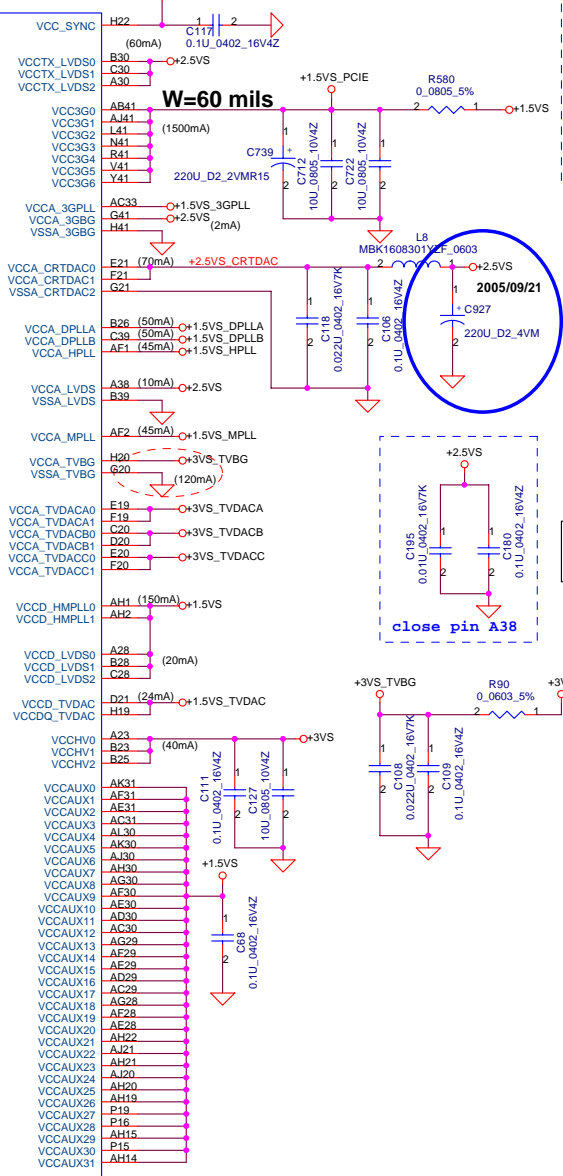
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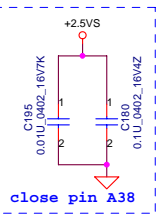
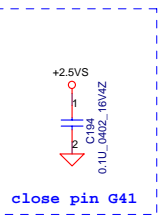
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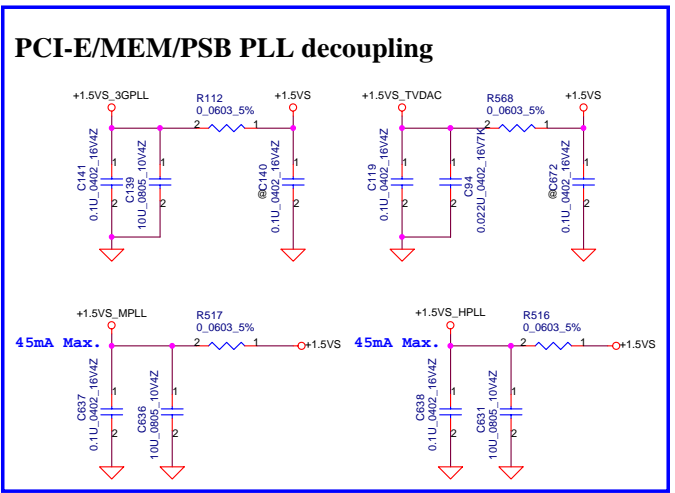
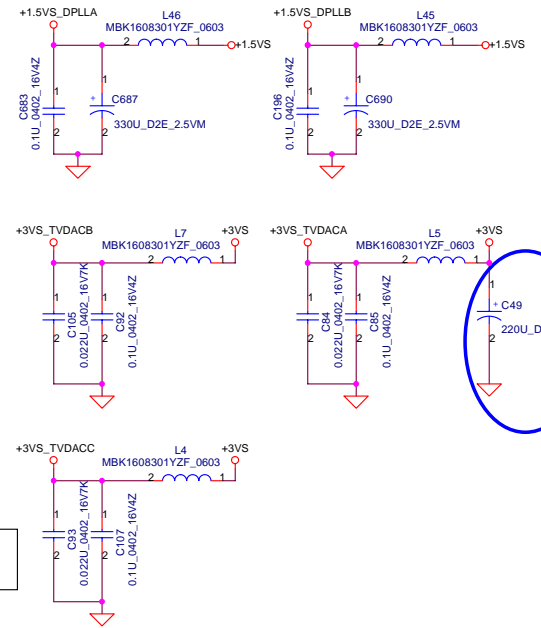
POWER



W=60 mils



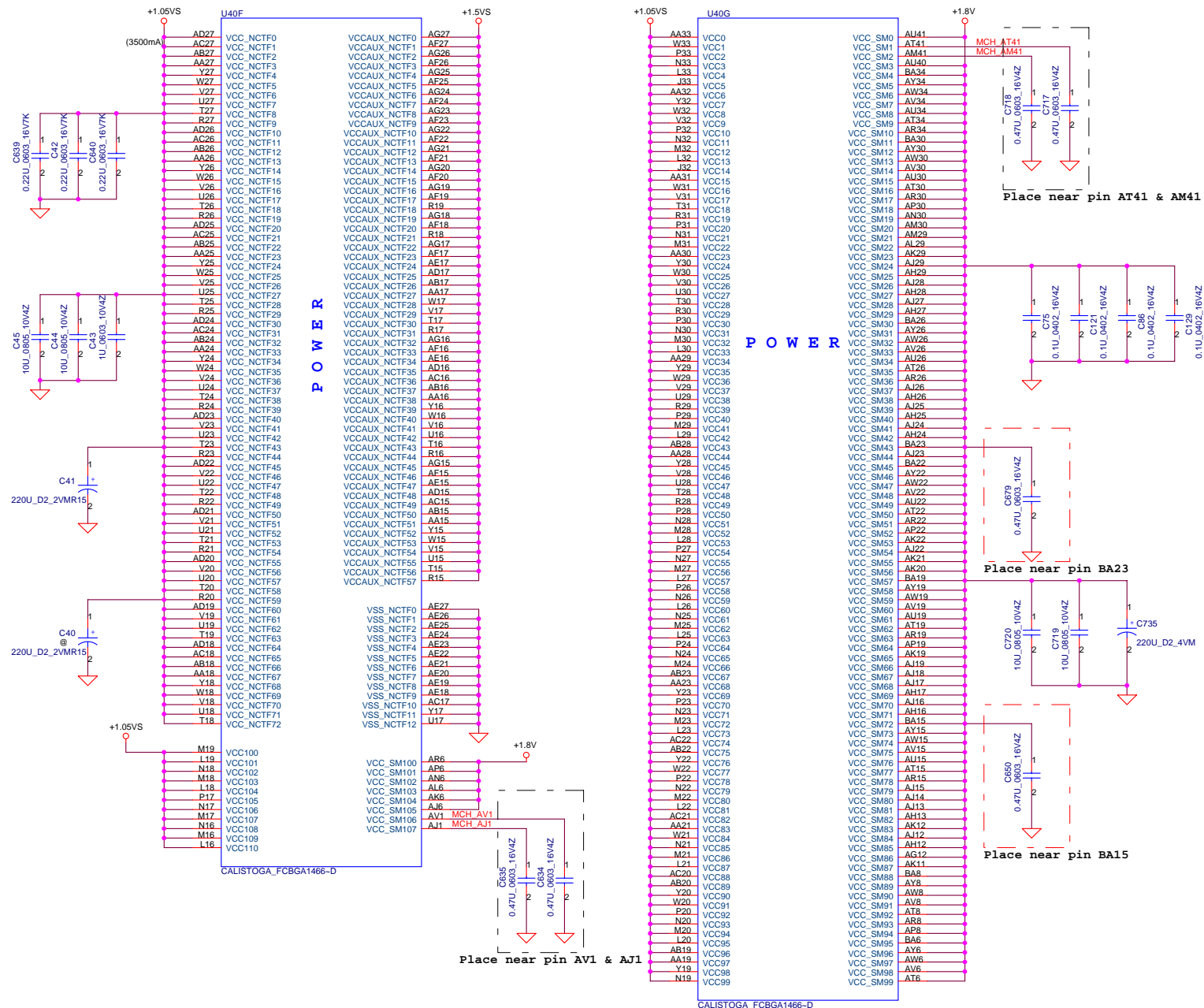
CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga



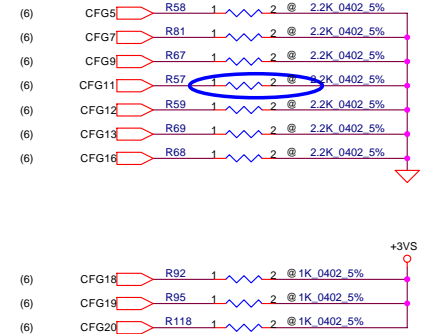
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Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

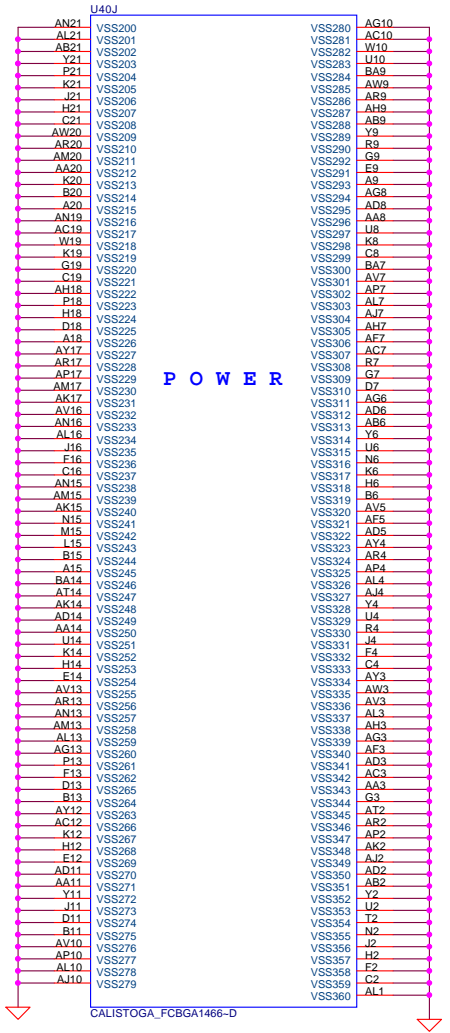
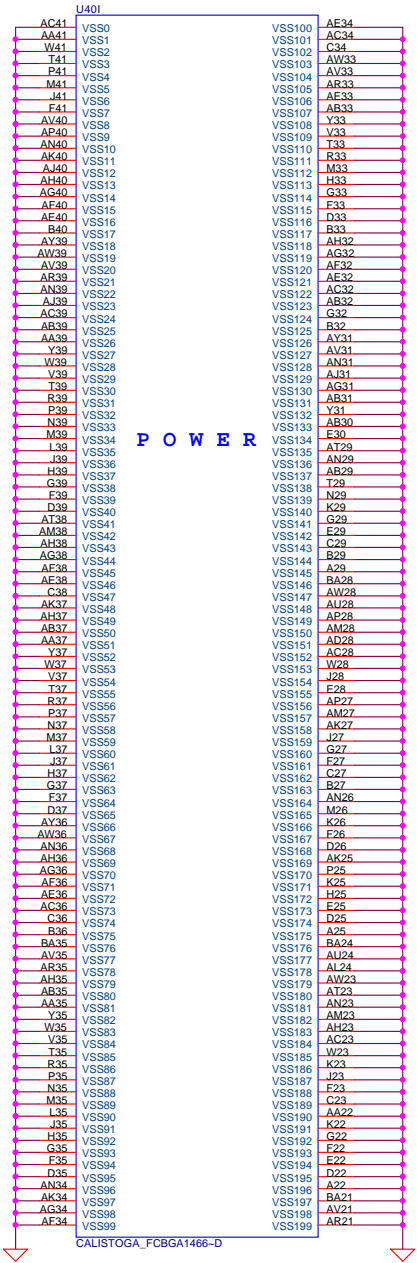


CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG6	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

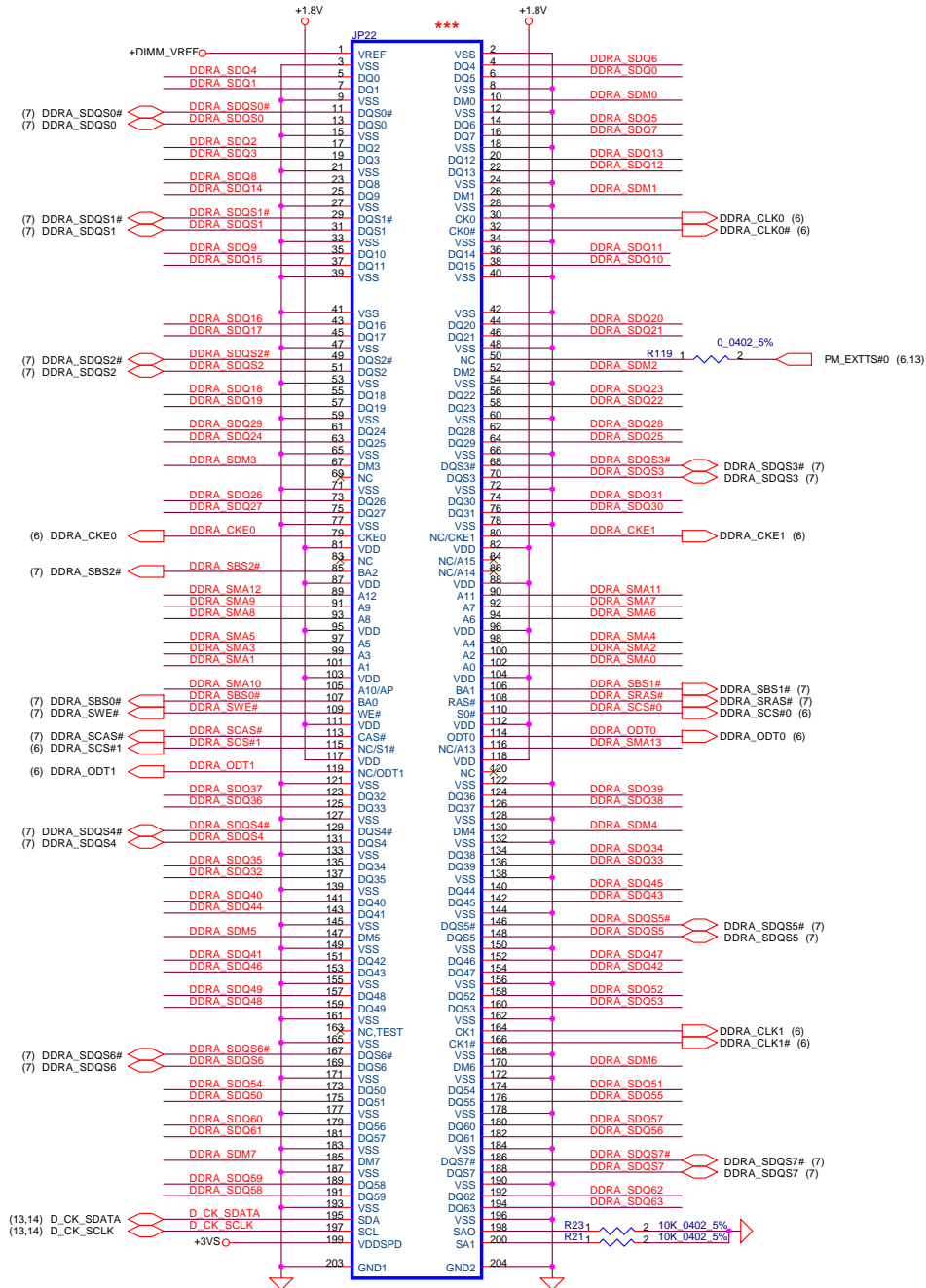


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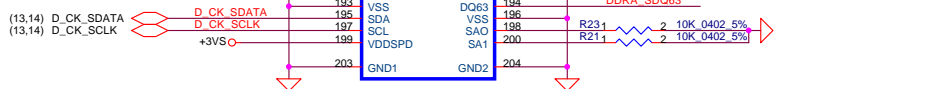
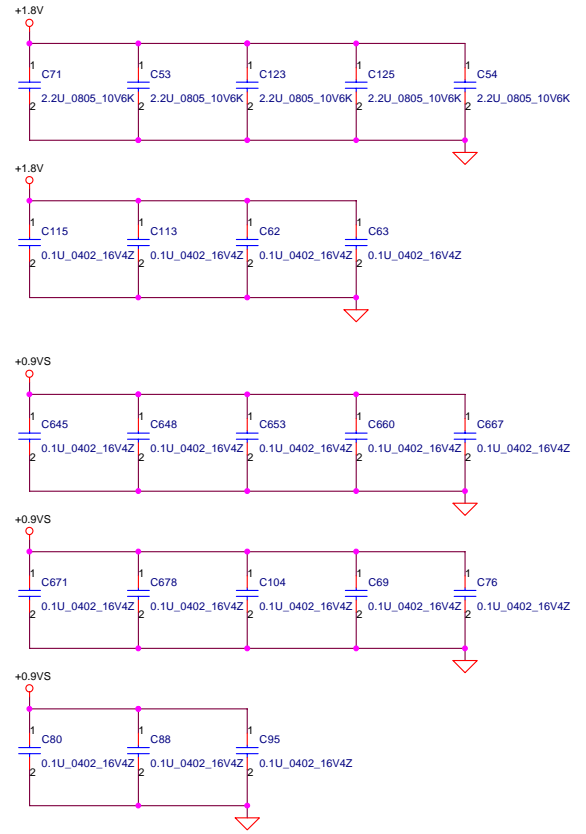
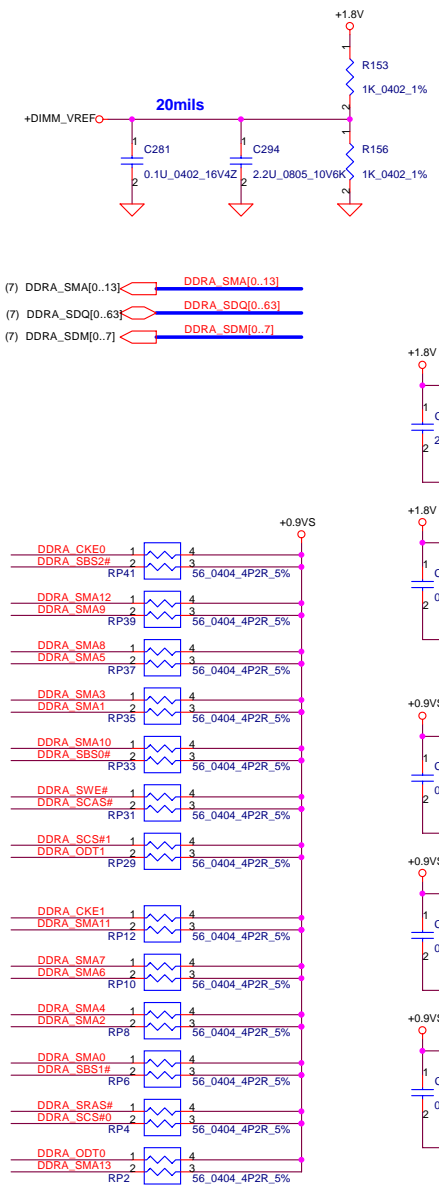


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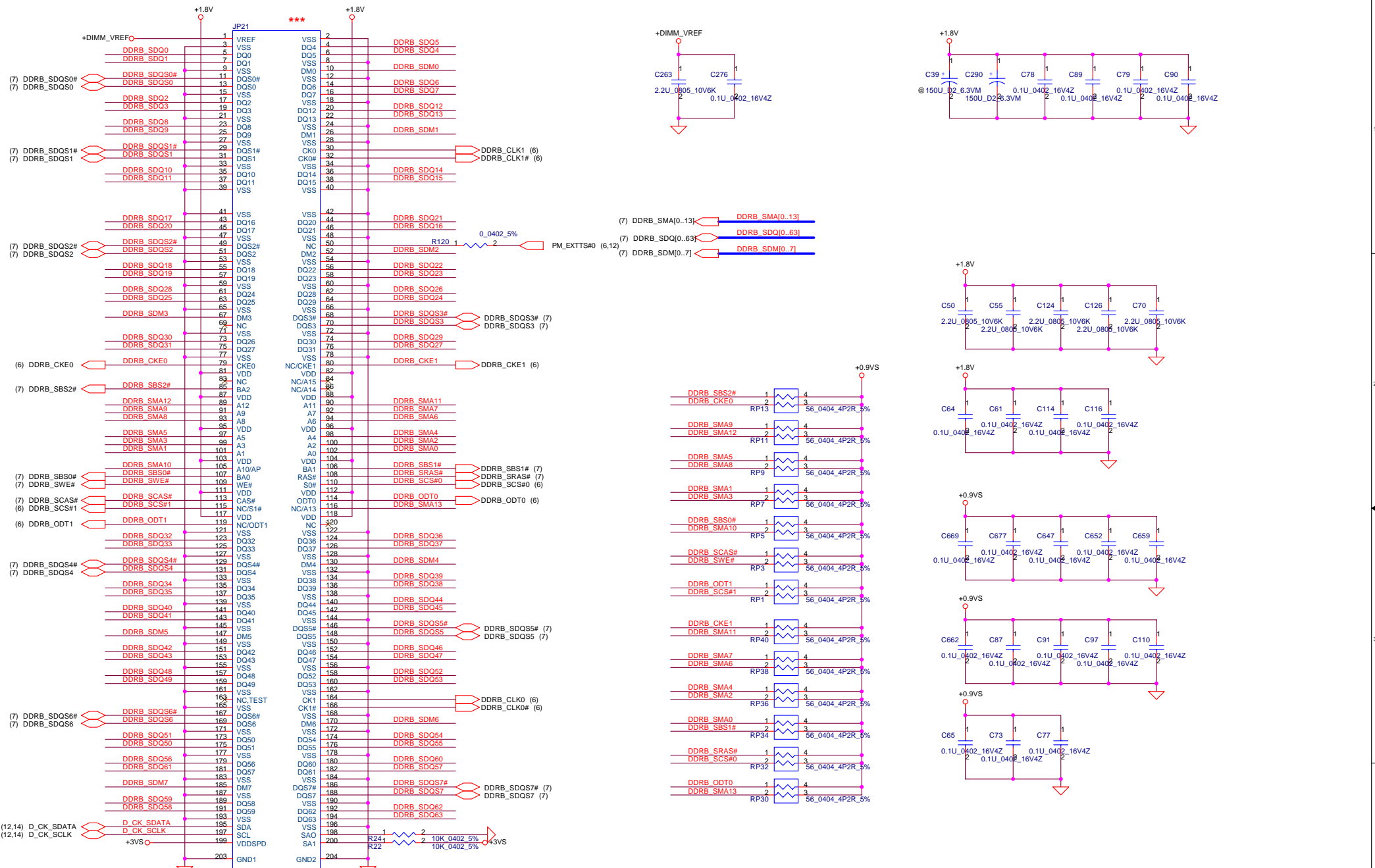


DIMM0 STD H:9.2mm (BOT)

P-TWO_A5692A-A0G16-N



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DIMM1 STD H:5.2mm (BOT)

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Size B	Document Number	Date:		Sheet	Rev
	HBL51 LA-3081P	Wednesday, November 09, 2005		13	0.2
				of	
				47	

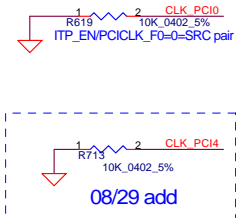
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

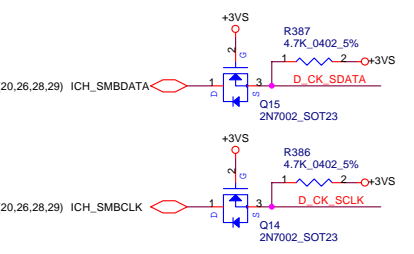
**SEL_PCI5=1=PCICLK5
ITP_EN/PCICLK_F0=0=SRC pair



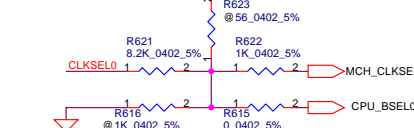
08/29 add



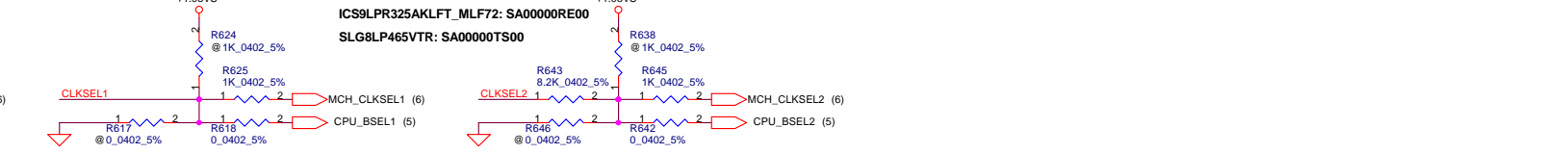
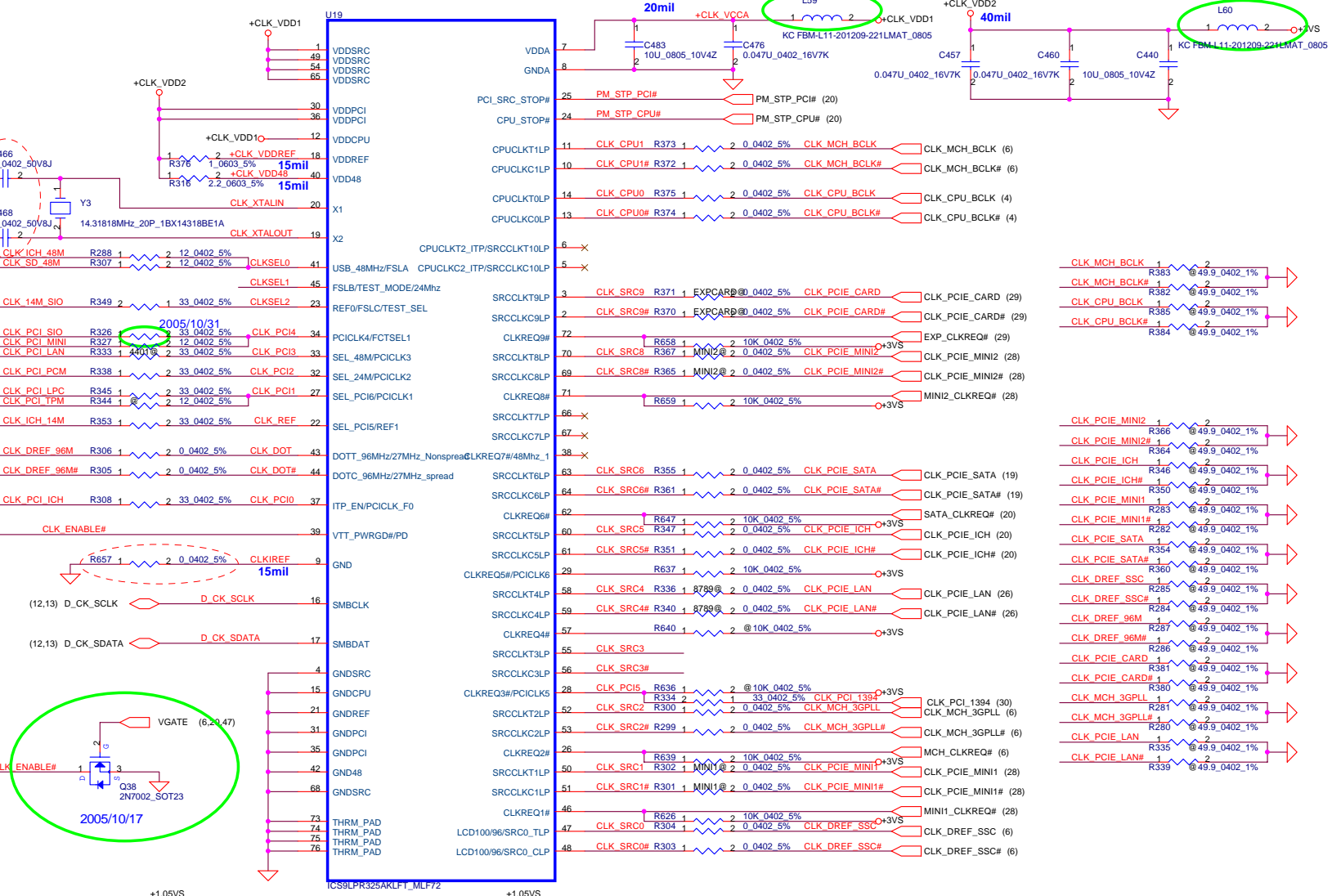
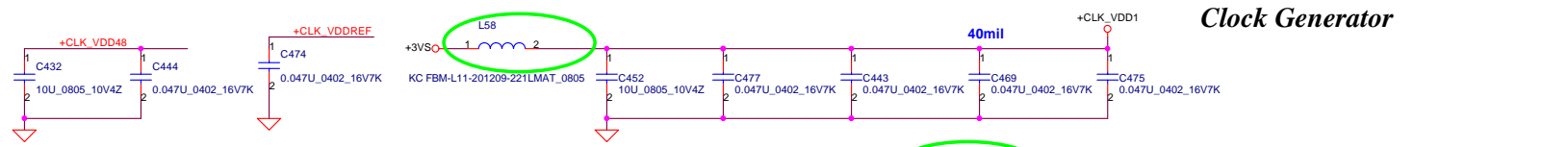
2005/10/17



2005/10/17



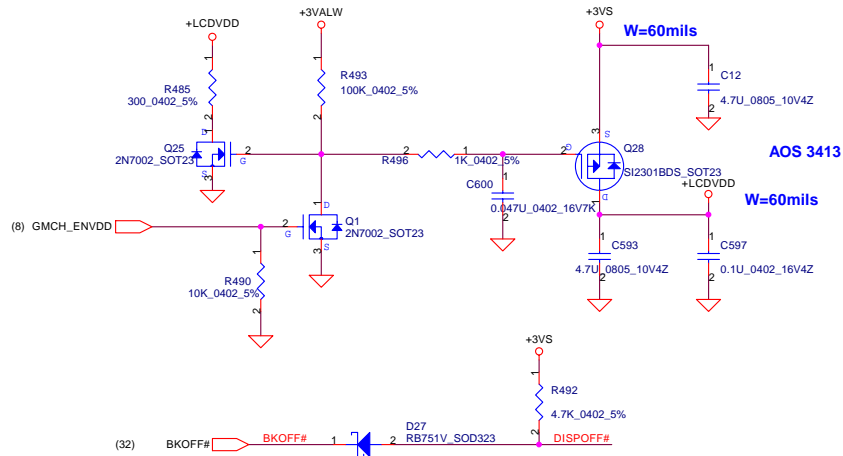
Clock Generator



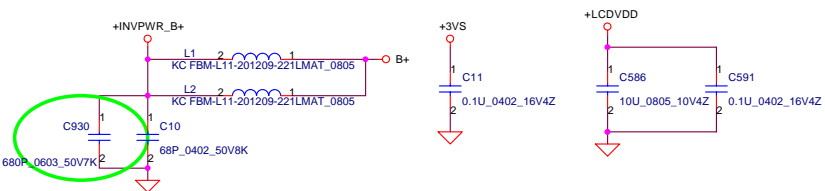
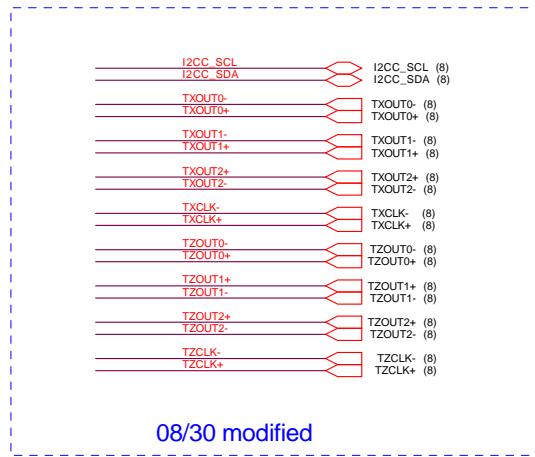
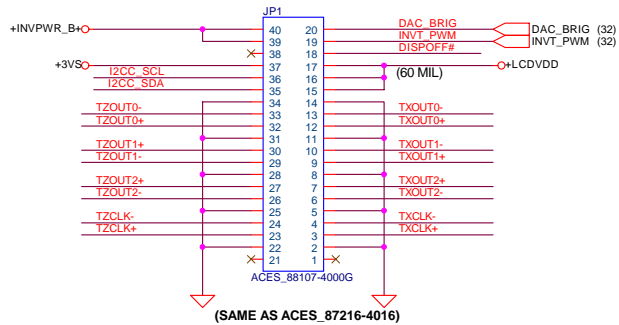
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Clock Generator			
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LCD POWER CIRCUIT

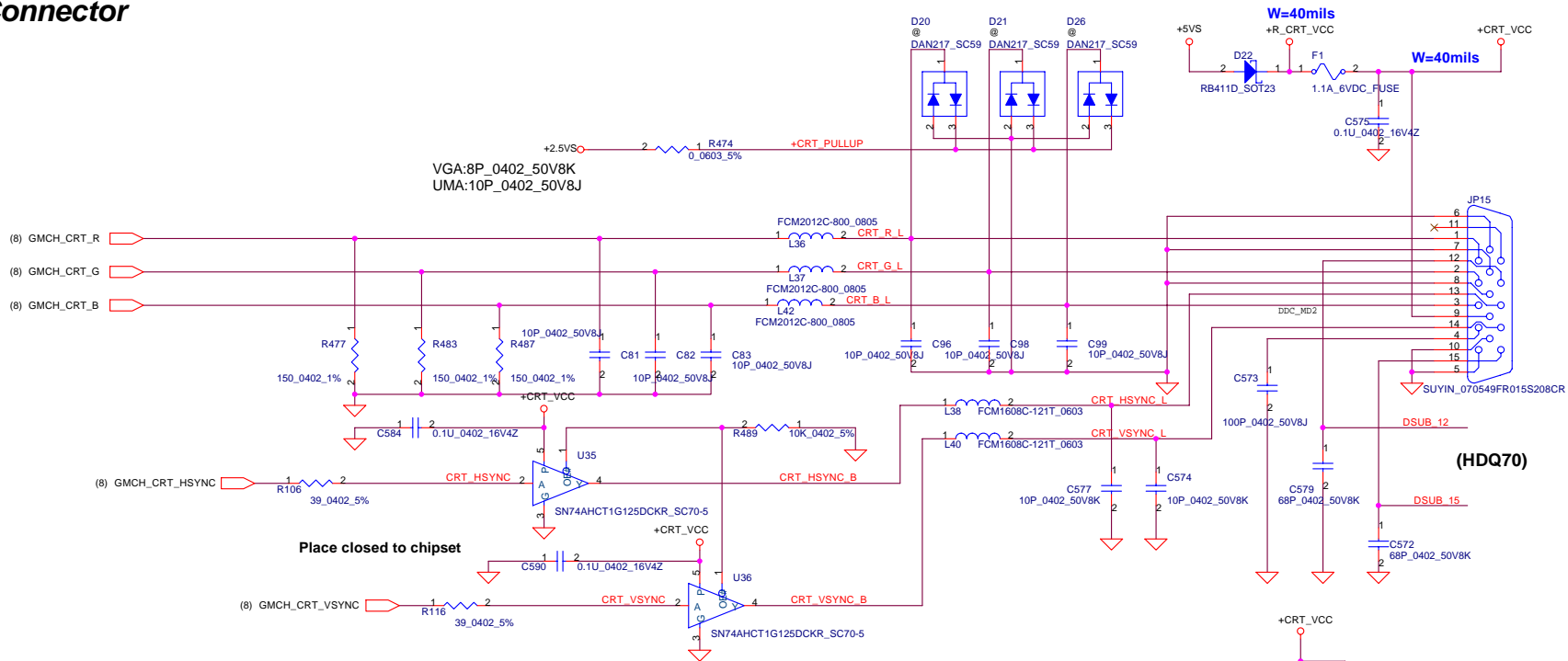


LCD/PANEL BD. Conn.

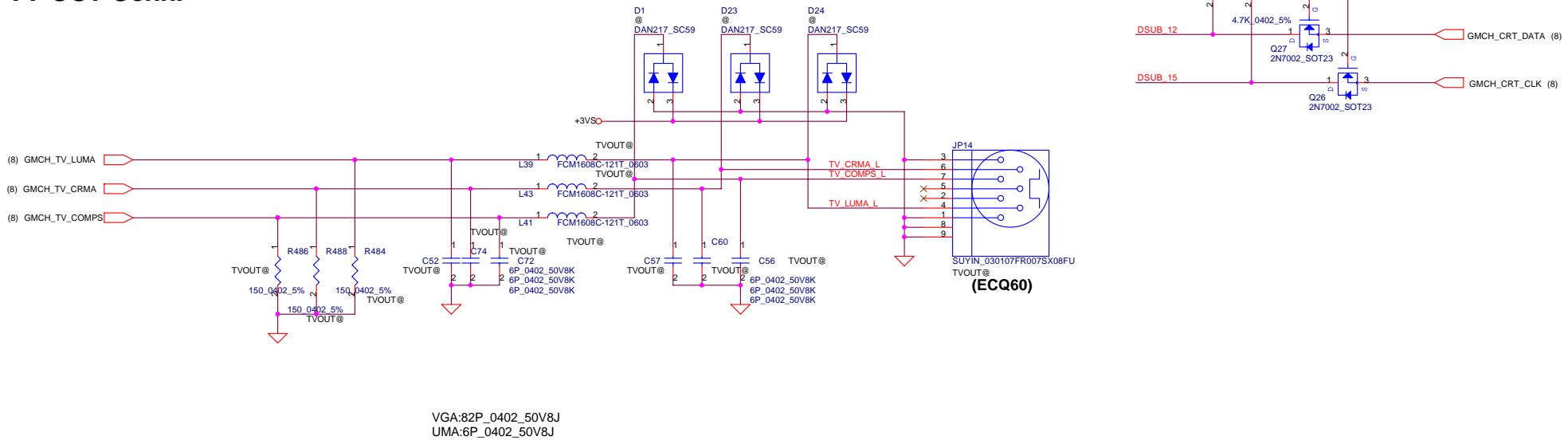


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				LCD Connector	
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				HBL51 LA-3081P	
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				Rev	0.2

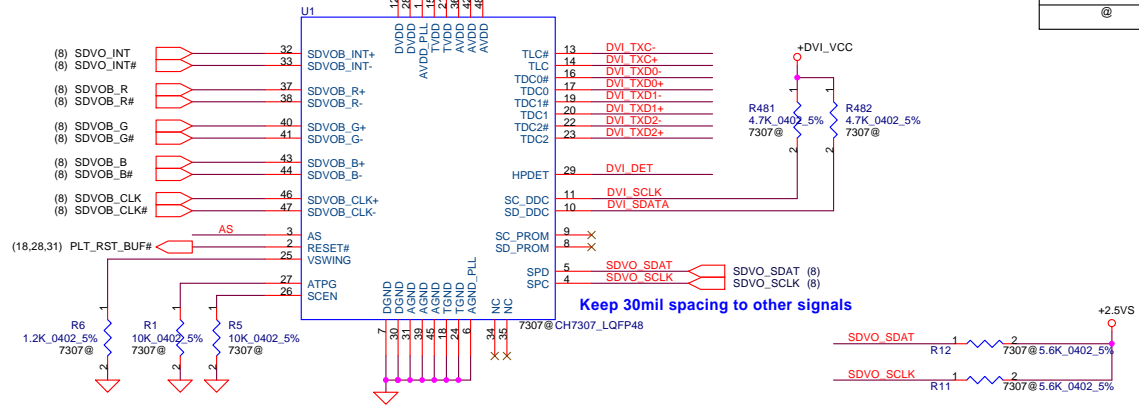
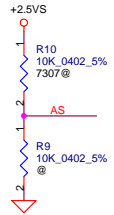
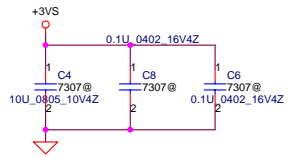
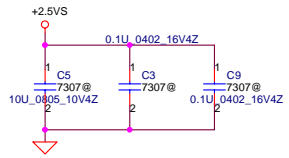
CRT Connector



TV-OUT Conn.

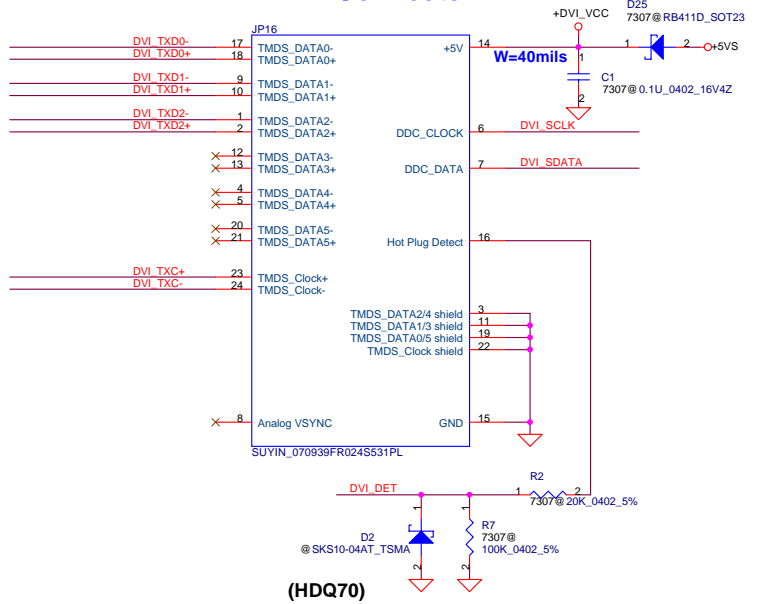


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Size B	Document Number	HBL51 LA-3081P		Rev	0.2
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BOM structure	DVI from SDVO
7307@	Stuff
@	No_Stuff

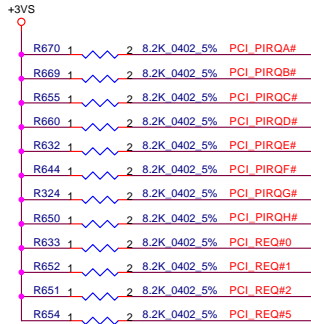
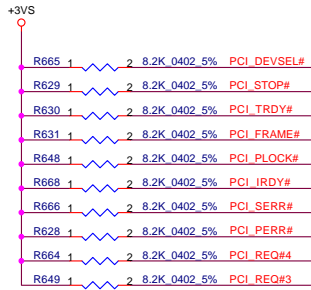
DVI-D Connector



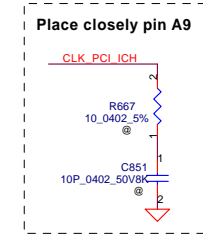
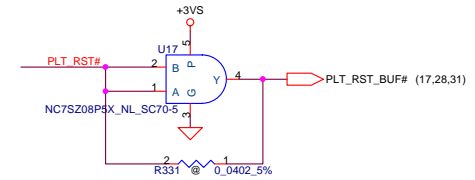
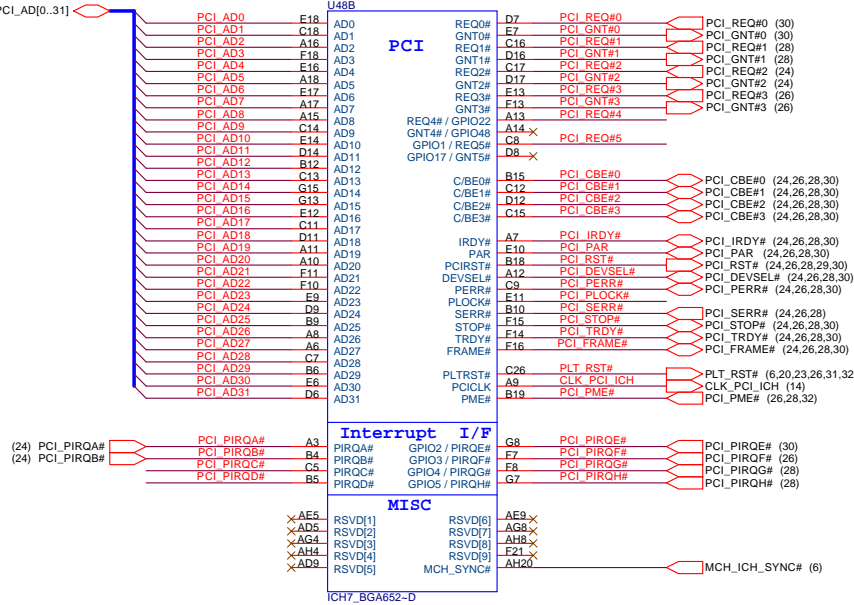
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				HBL51 LA-3081P	
				Date:	Wednesday, November 09, 2005
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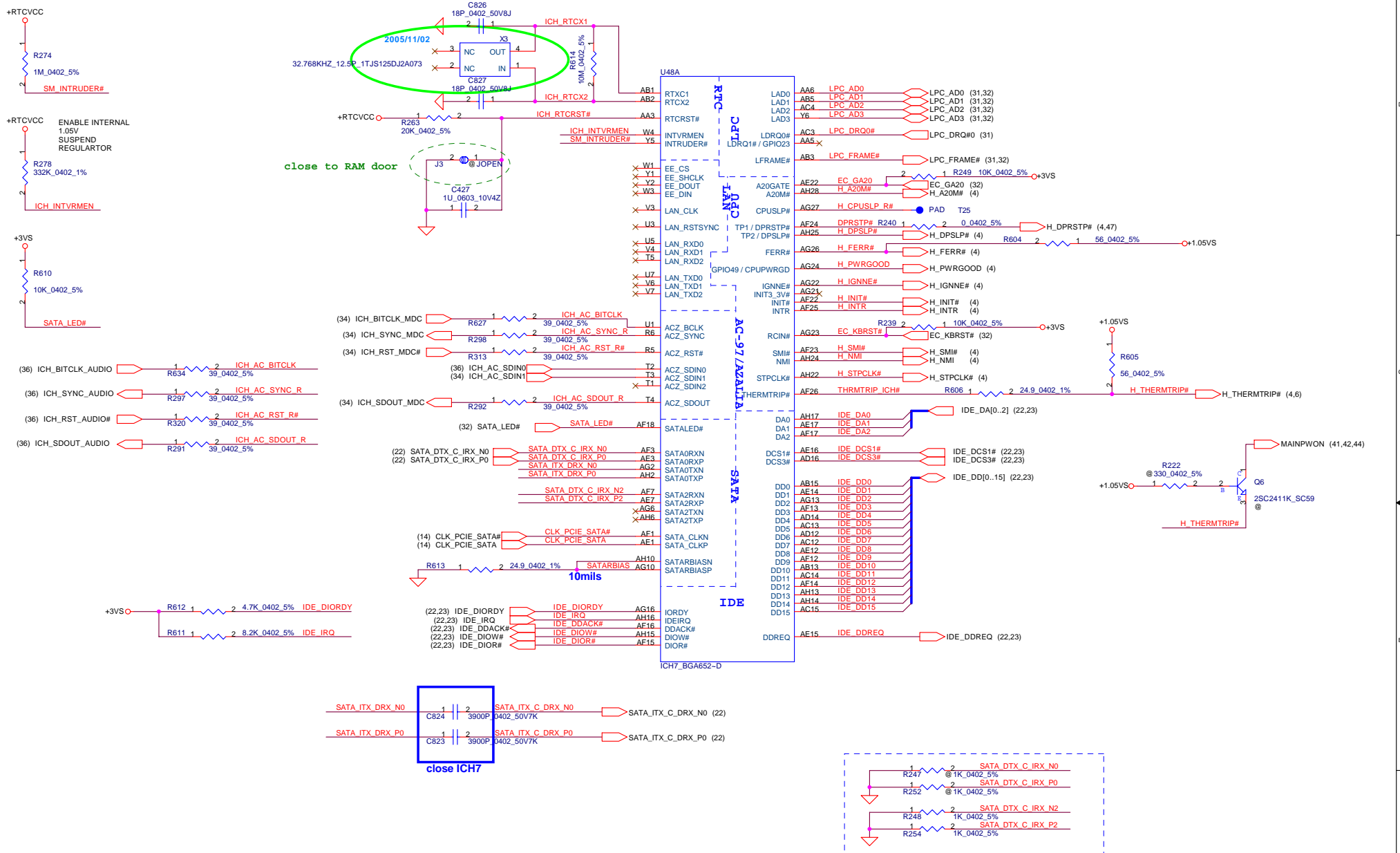
Compal Electronics, Inc.	
Size B	Document Number
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ICH7M(B-0) (QK17) [ES3] : SA00000JK30



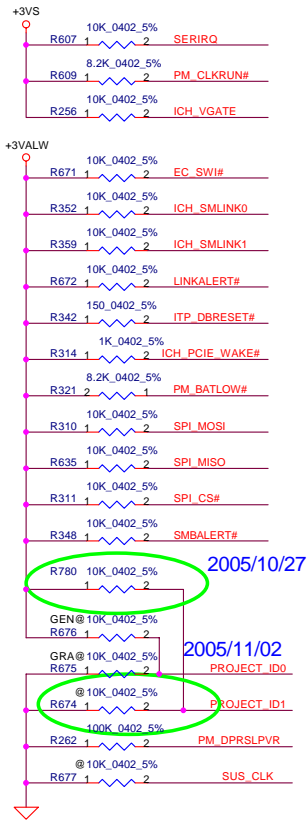
(24,26,28,30) PCI_AD[0..31]





SATA_RxN/p need tie to ground when SATA port no used

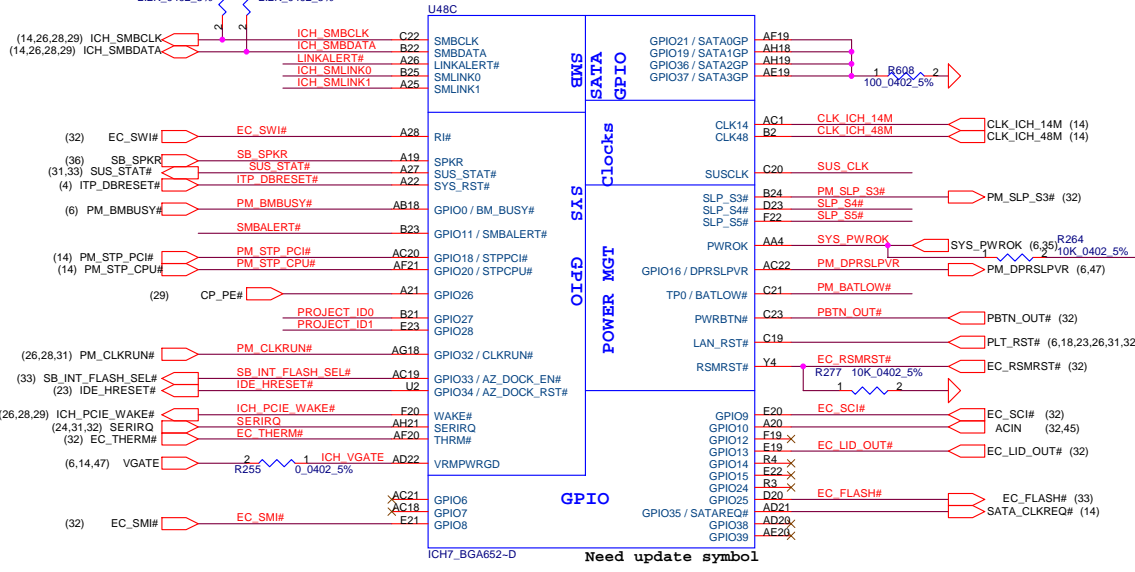
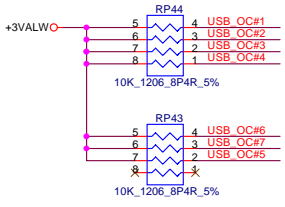
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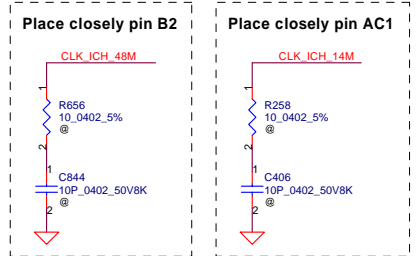
2005/10/27

2005/11/02

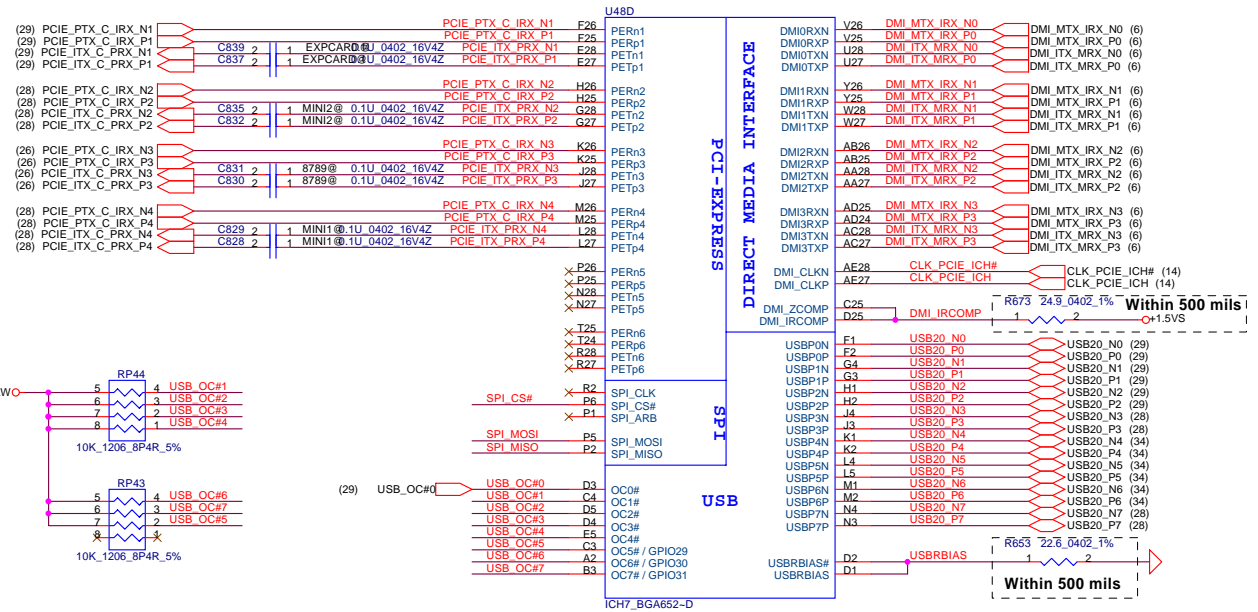
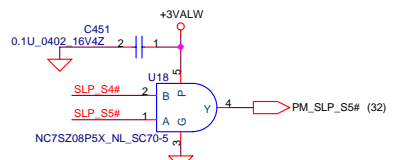
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00	= Grapevine
01	= Geneva
10	= HBL51_PATA



Need update symbol



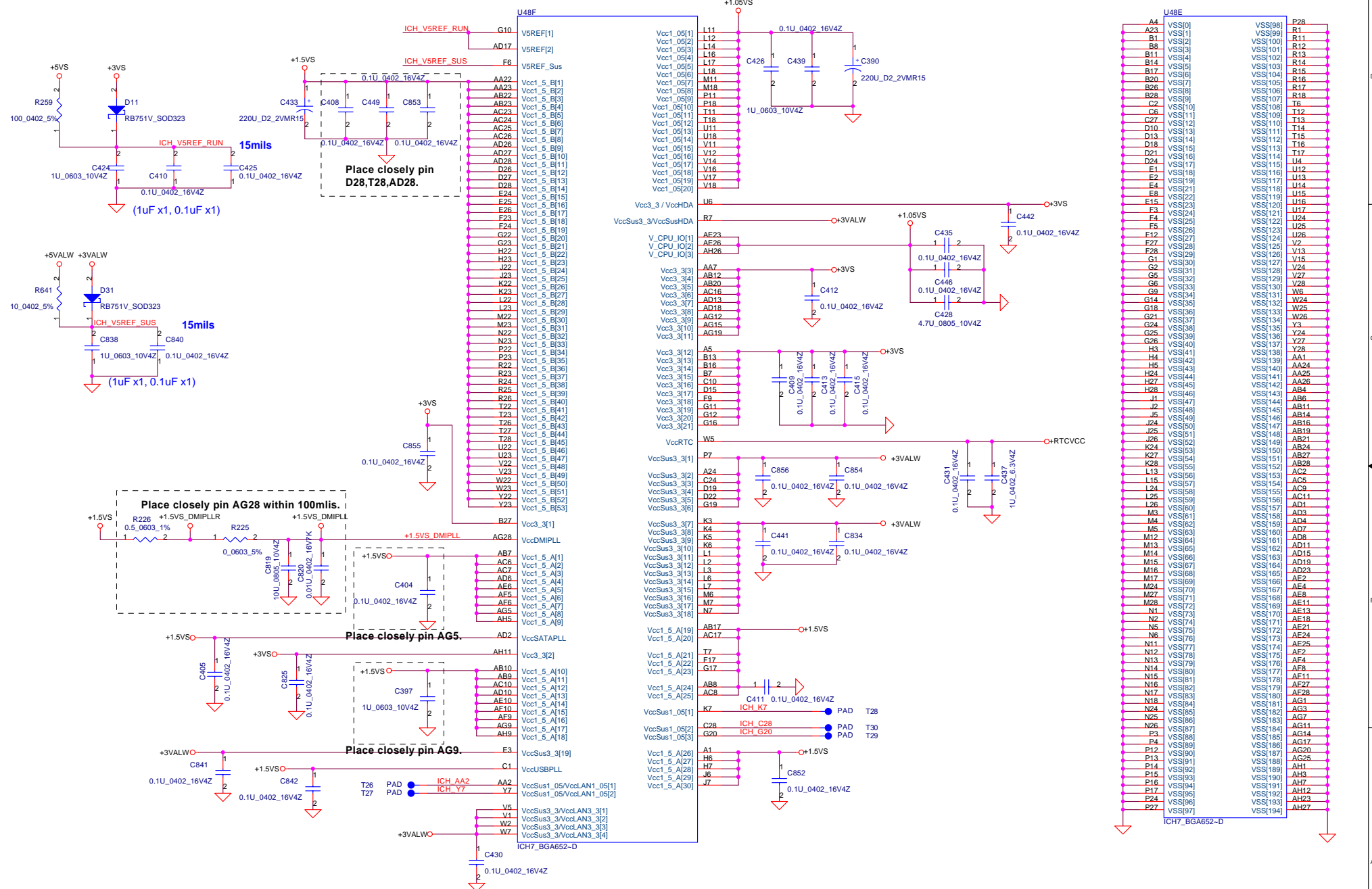
PM_DPRSPLPVR : Need to series a 500Ohm resistor to IMVP6



Within 500 mils

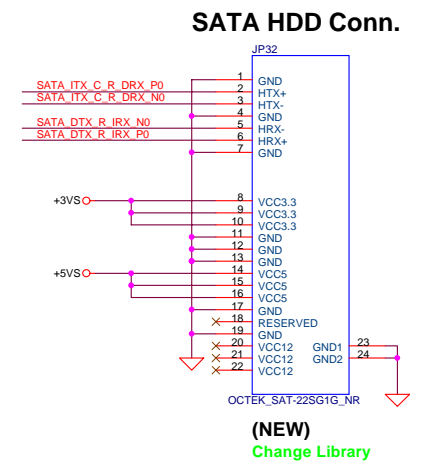
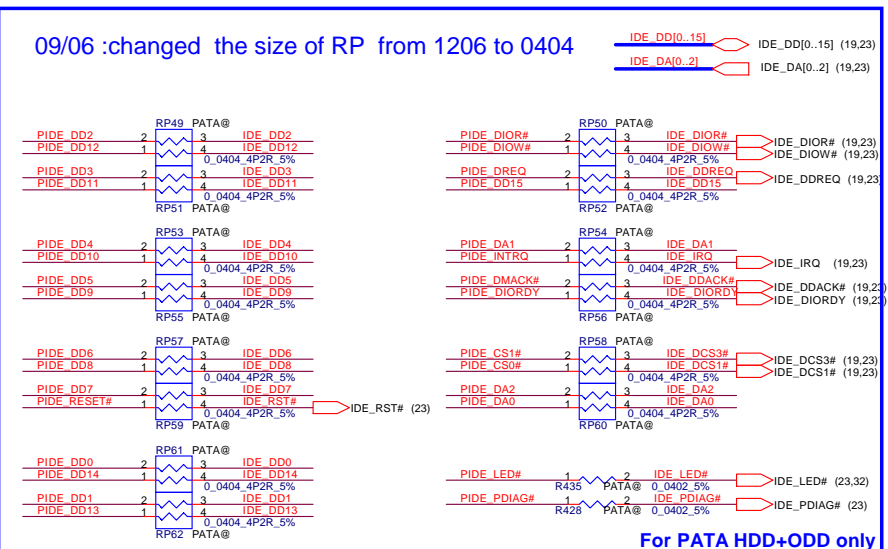
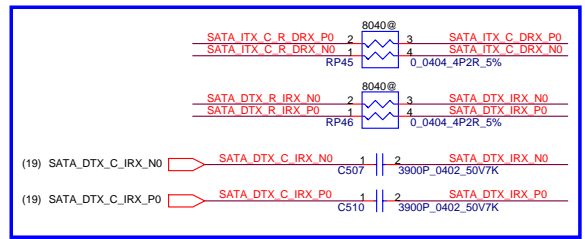
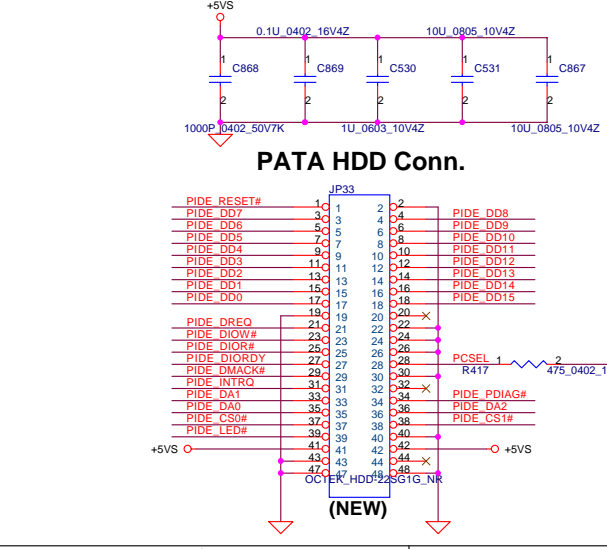
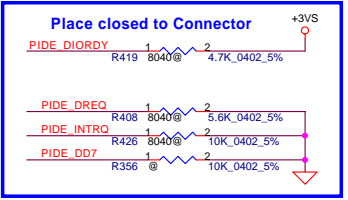
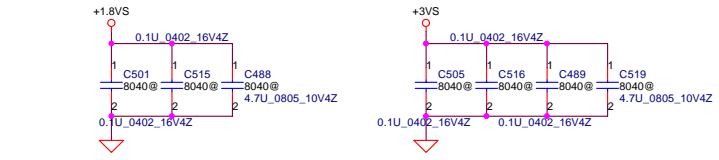
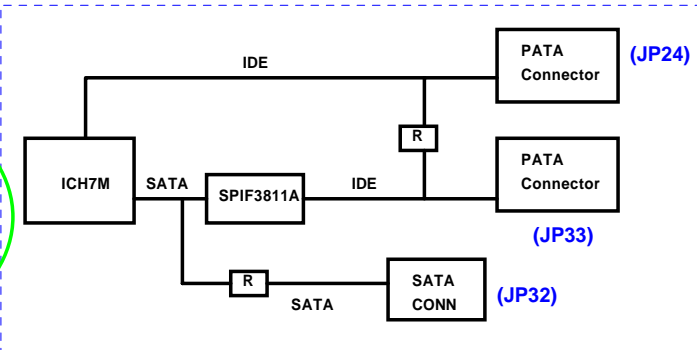
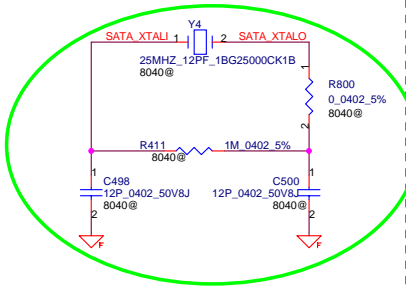
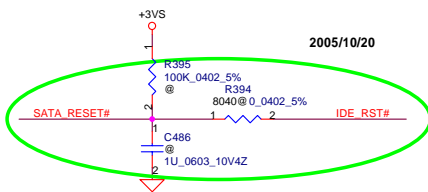
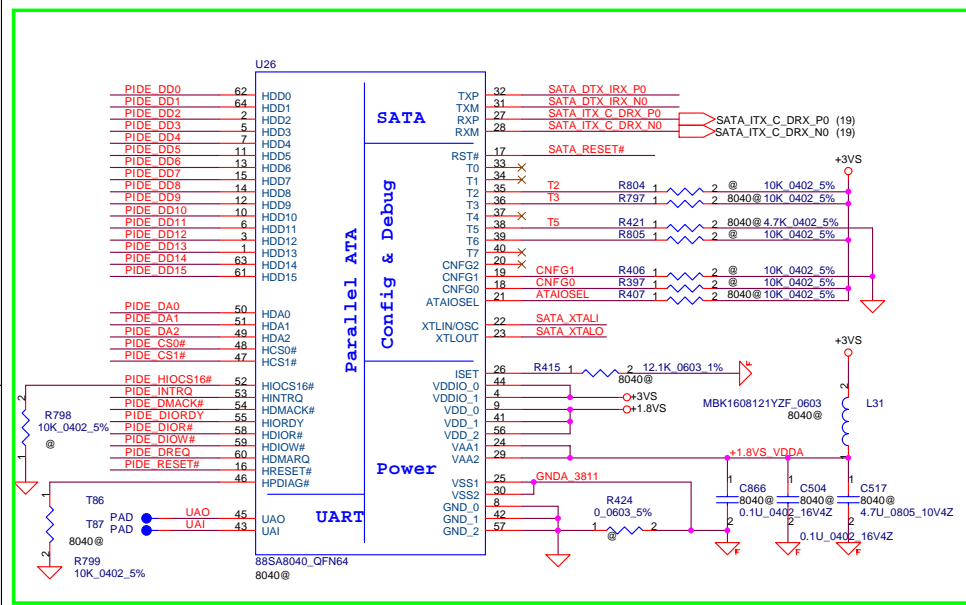
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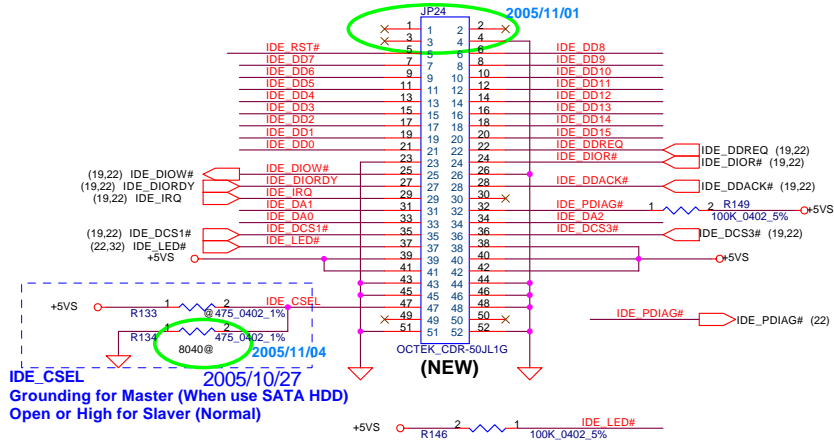
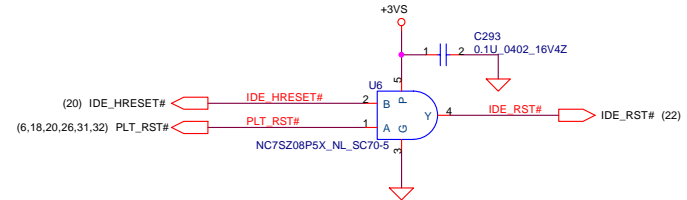
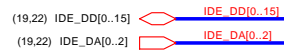
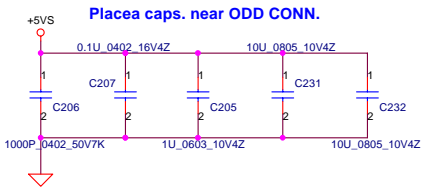
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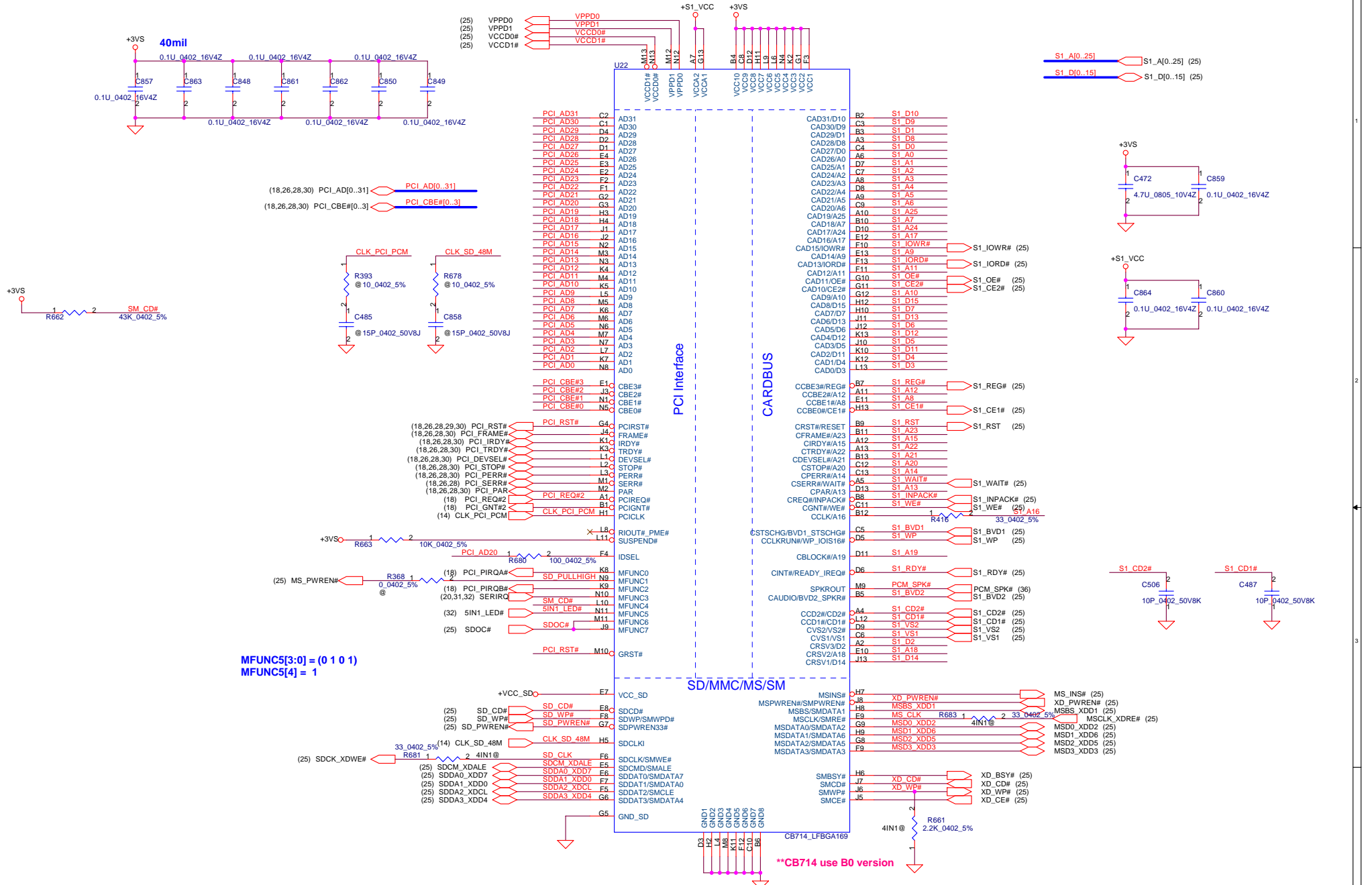
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Title			
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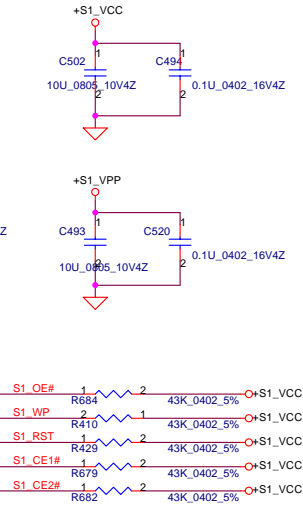
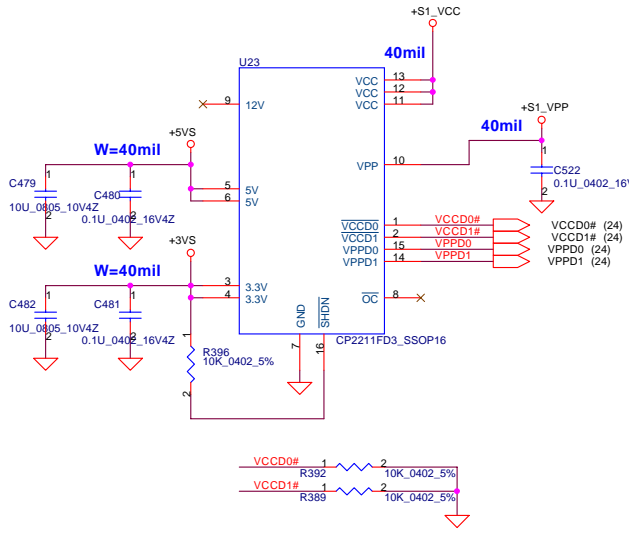


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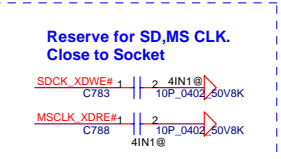
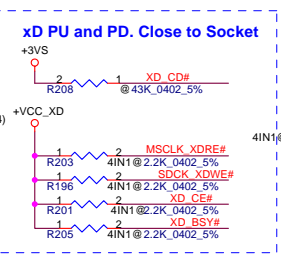
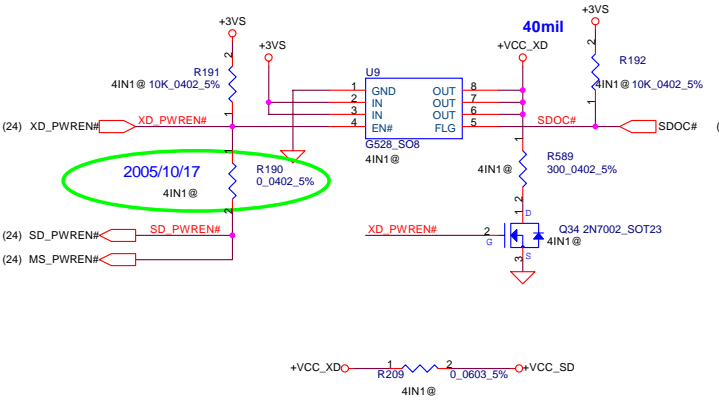


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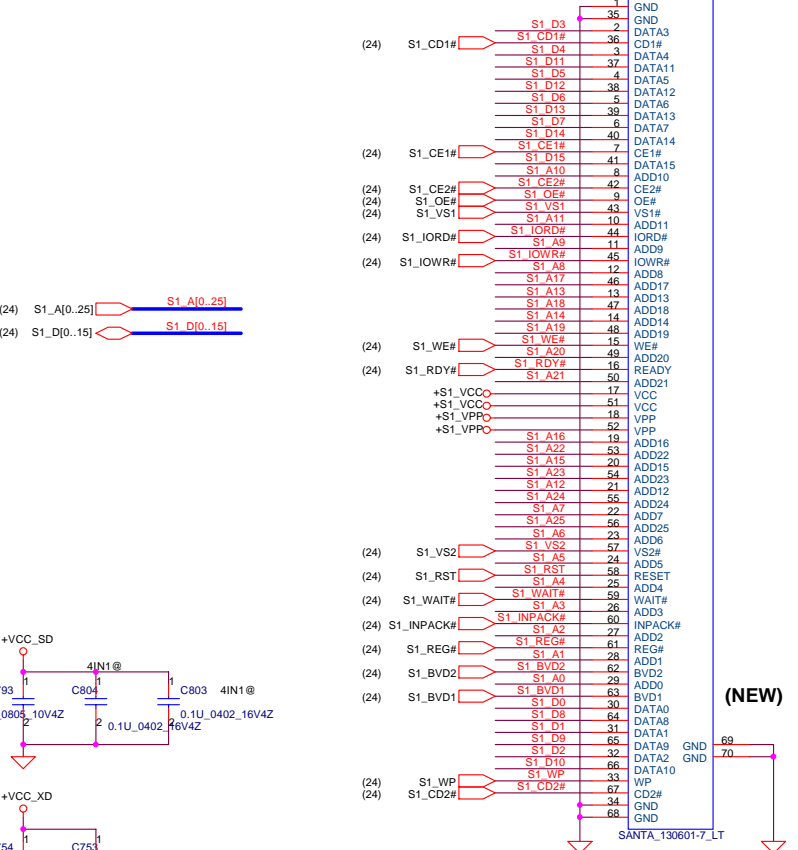
PCMCIA Power Control



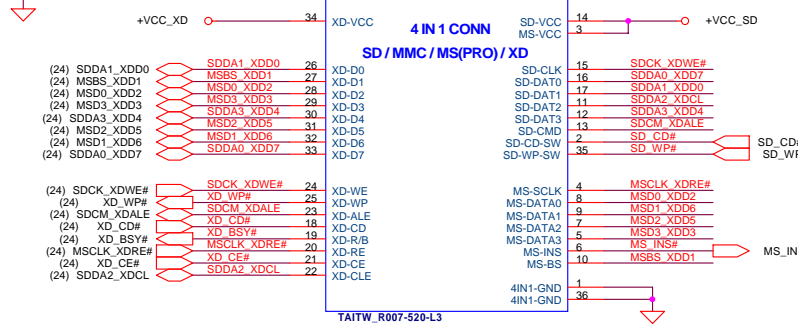
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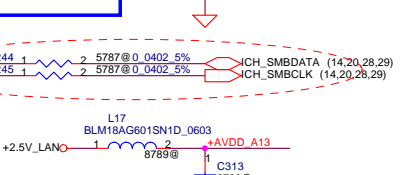
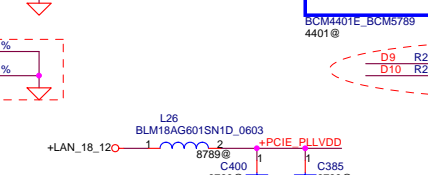
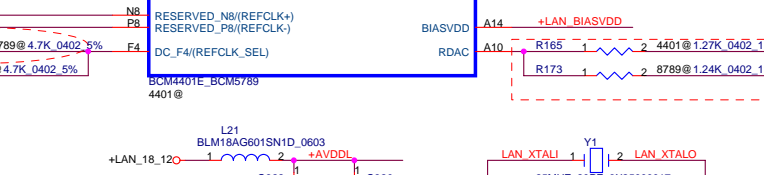
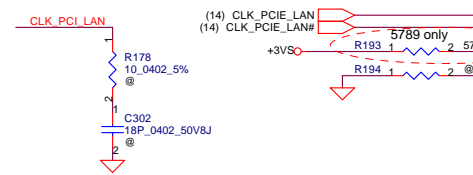
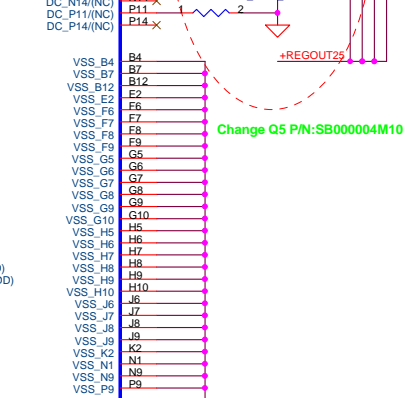
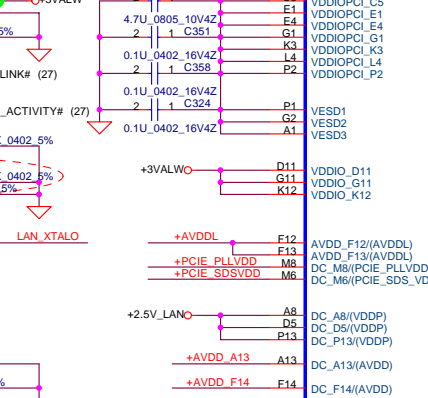
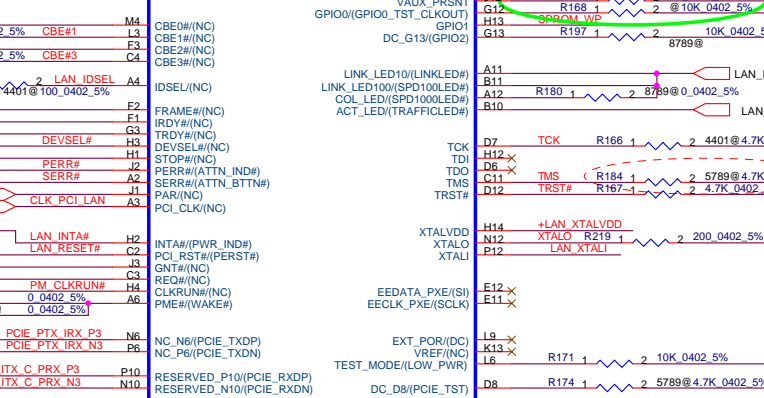
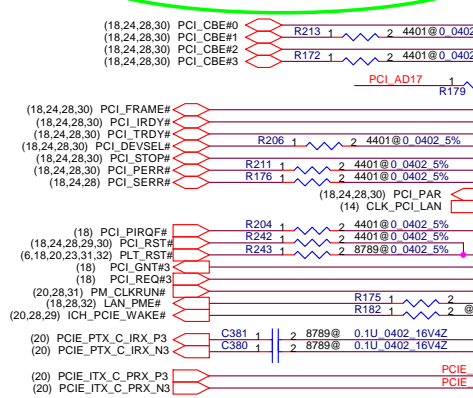
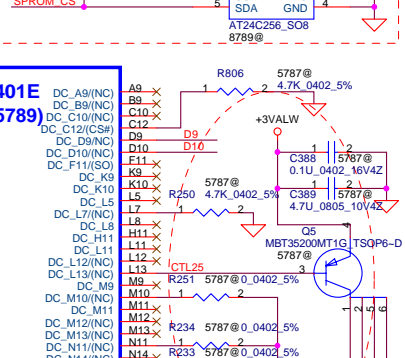
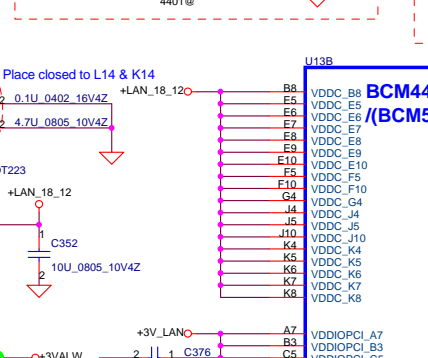
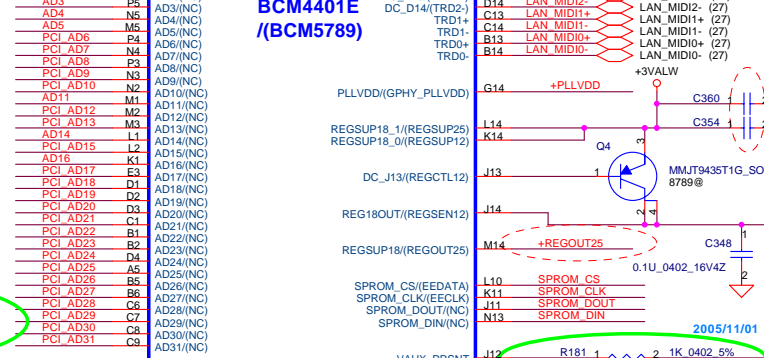
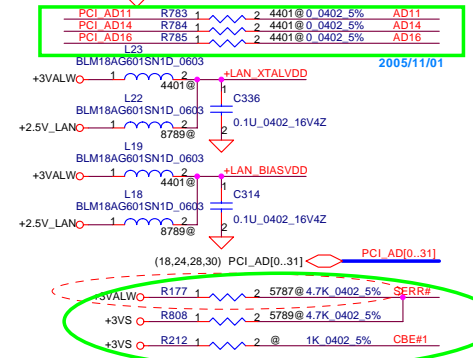
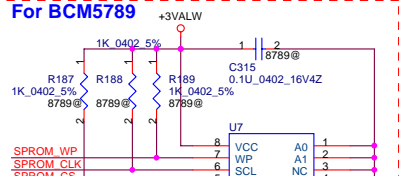
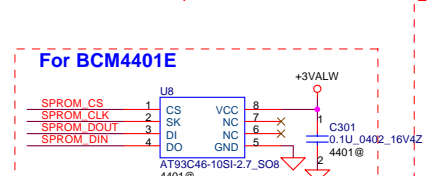
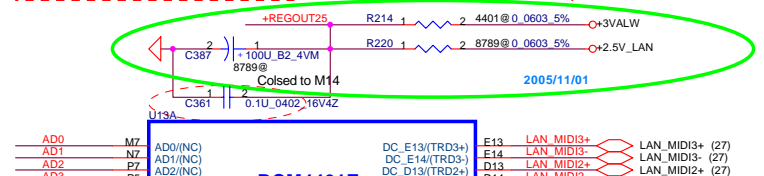
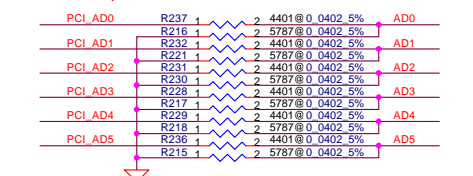
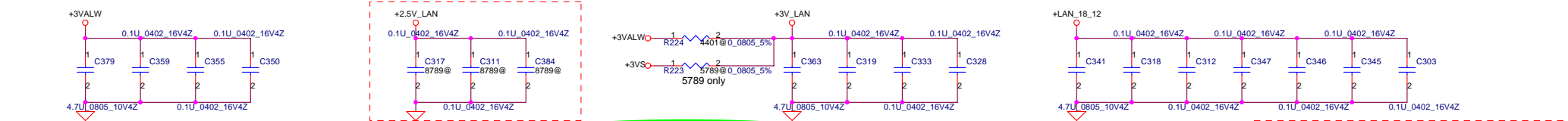
PCMCIA Socket



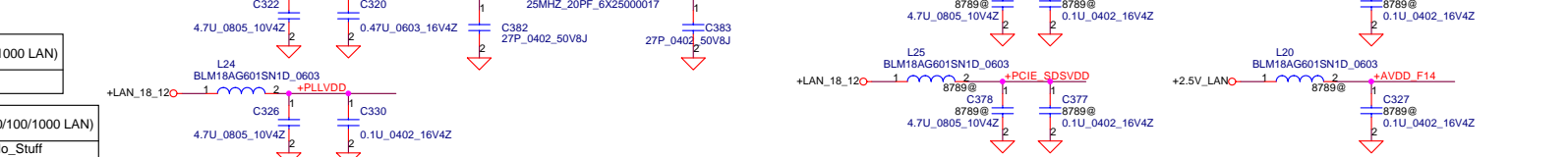
4 IN 1 Socket (HDQ70)



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	(SA00000D10)	(SA00000SZ00)	
FN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K



BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

Security Classification		Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date	2006/06/20

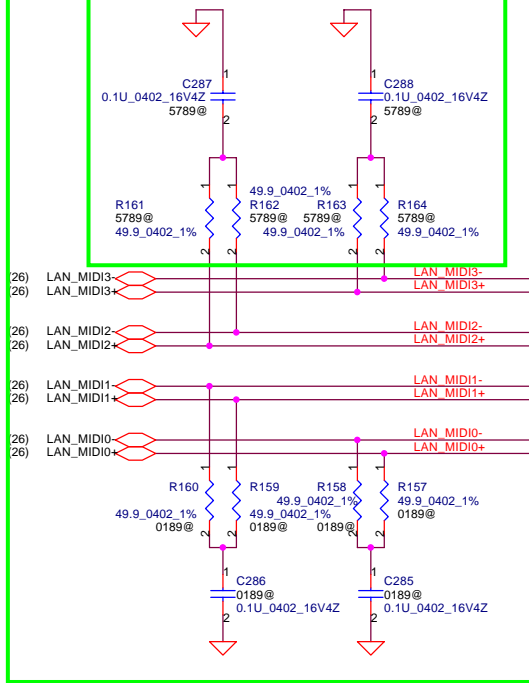
Compal Electronics, Inc.			
LAN BCM4401E/Jade15			
Size	Document Number	Rev	
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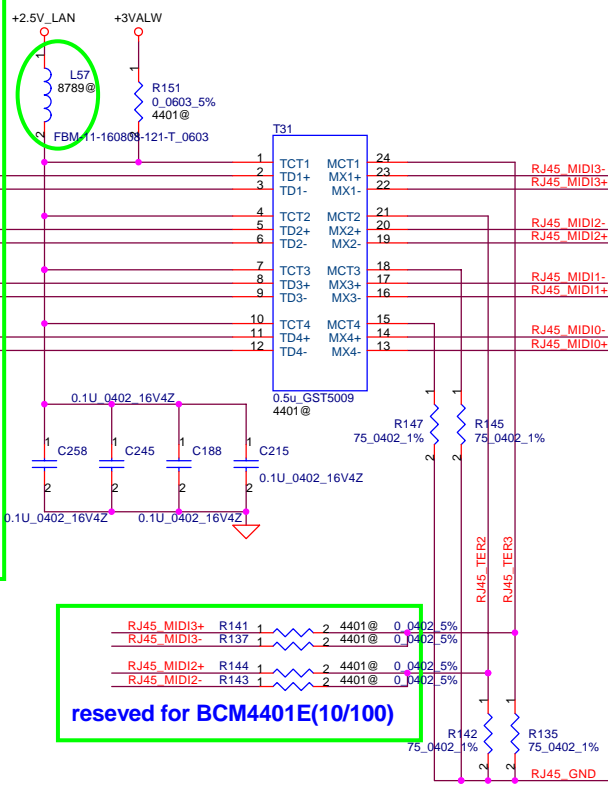
LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)

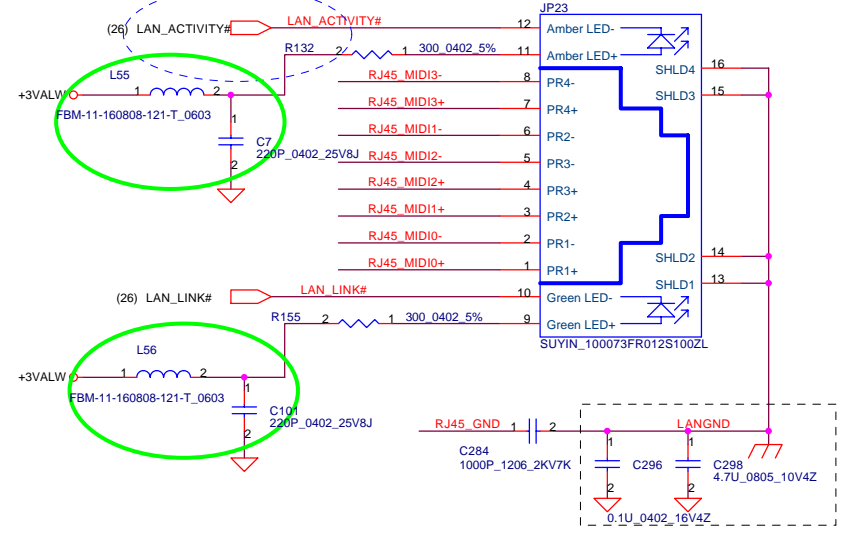


GbE Transformer: GST5009 (SP050005610)
10/100 Transformer : TST1284-LF (SP050001X10)

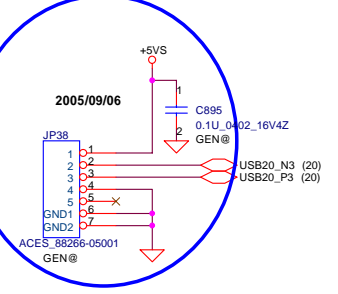
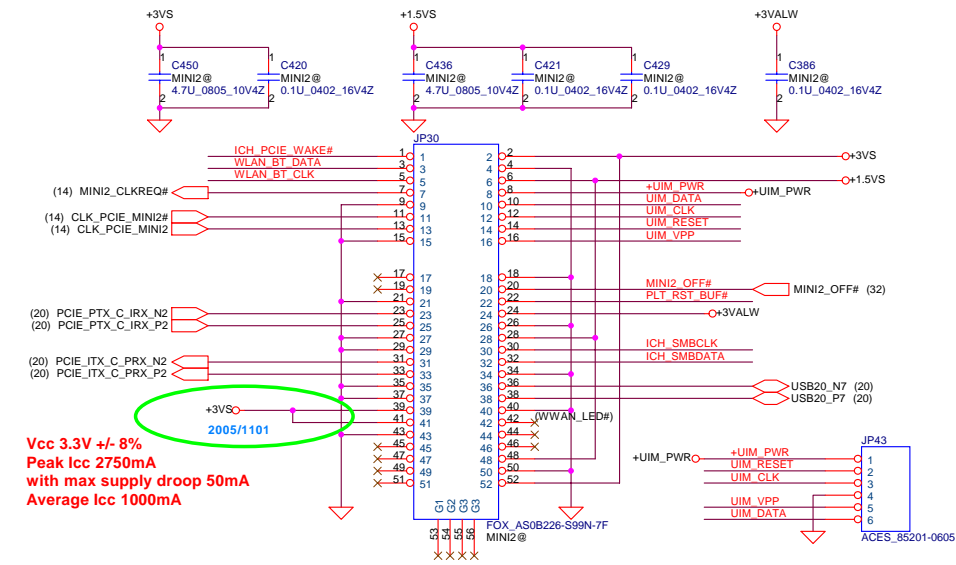
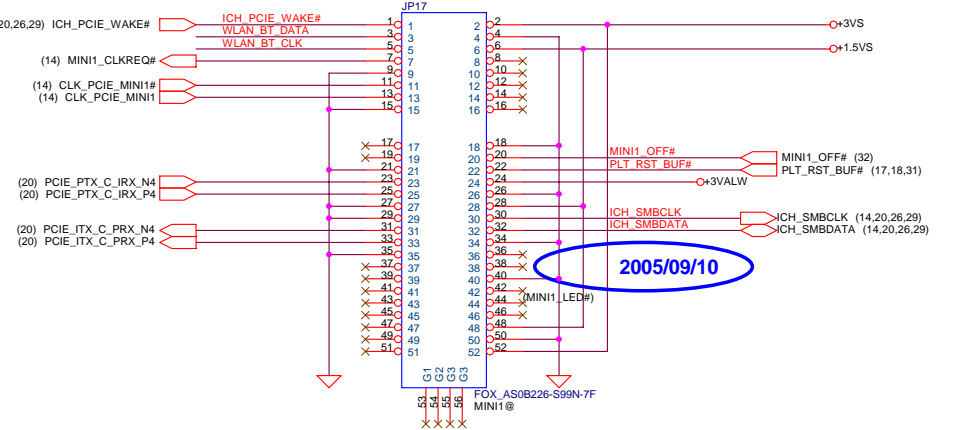
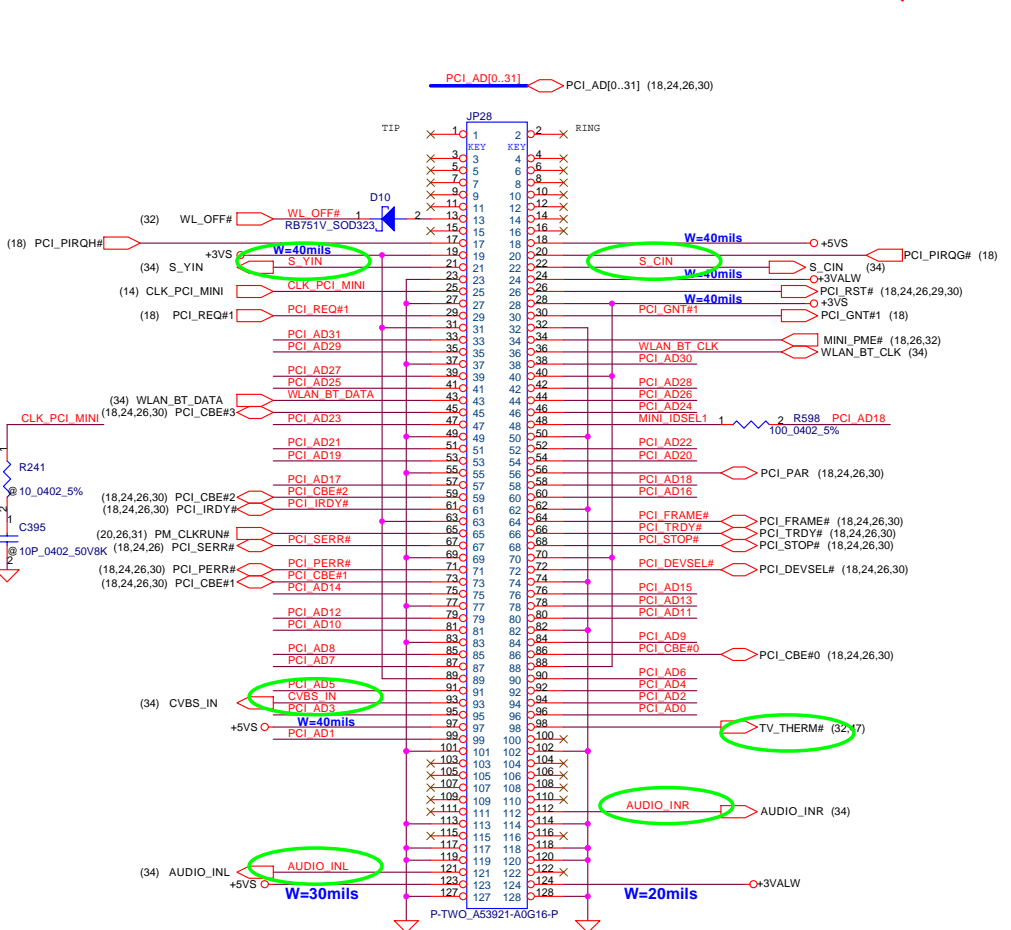
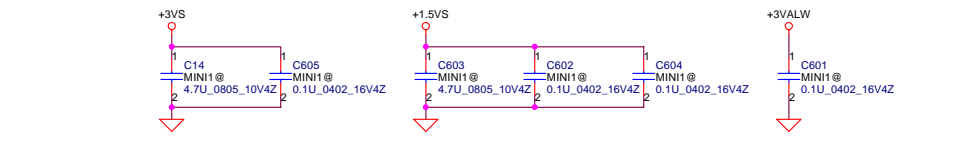
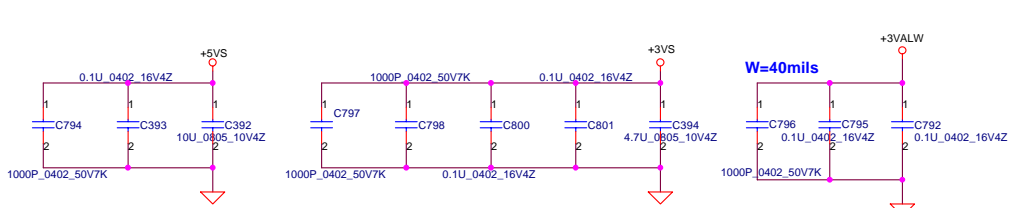


reserved for BCM4401E(10/100)

09/06 modified (symbol must be updated)

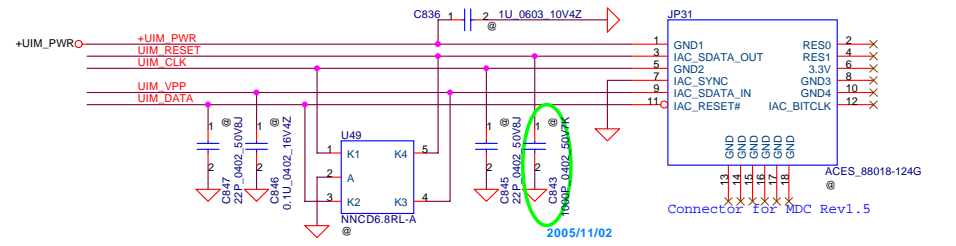


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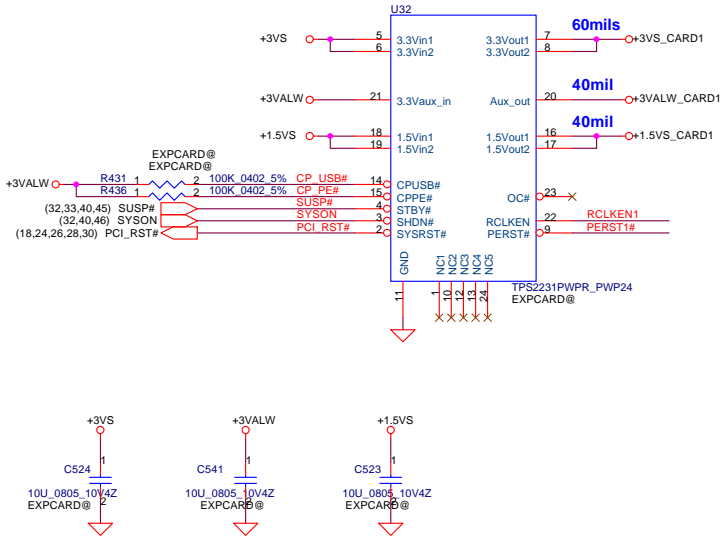


(Change to SP070003200)

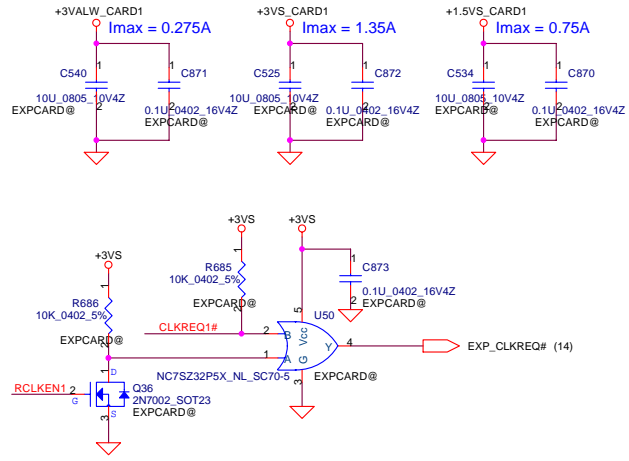
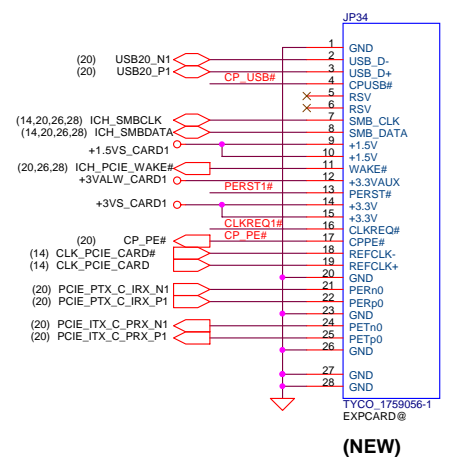
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



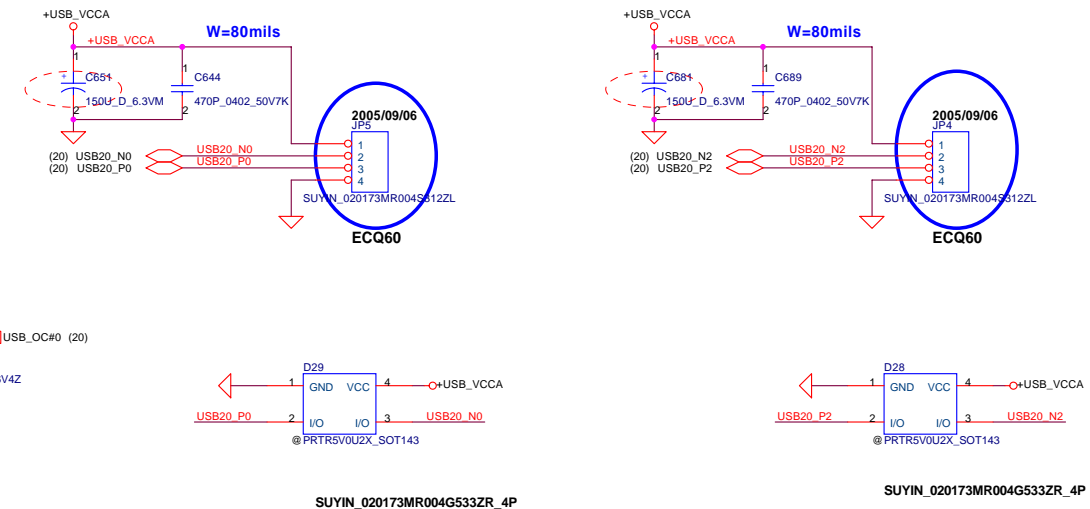
New Card Power Switch



New Card Socket (Left)

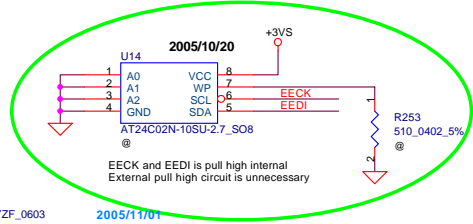
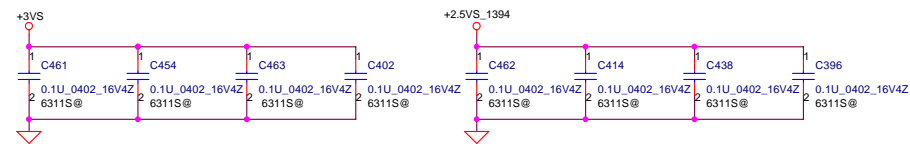


USB CONN. 1 & 2

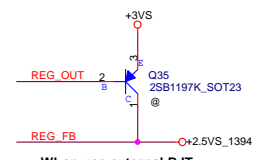
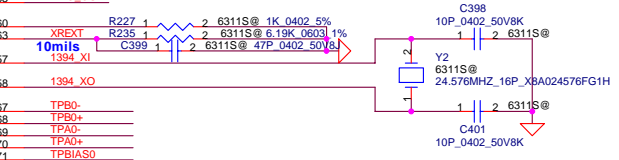
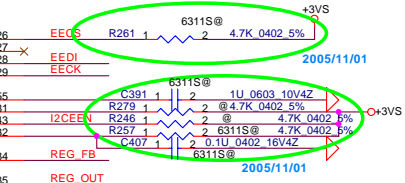
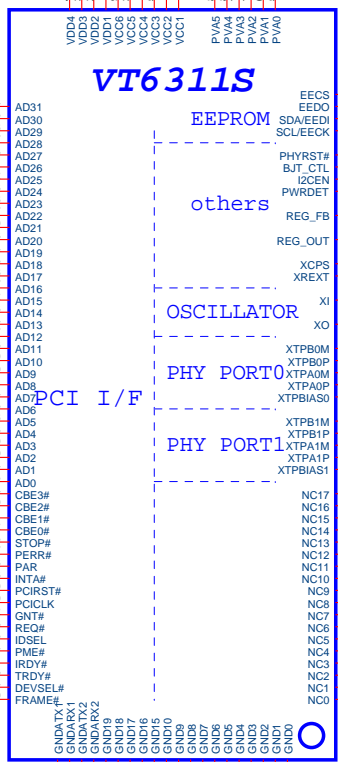
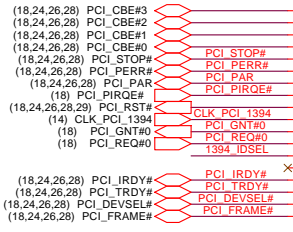
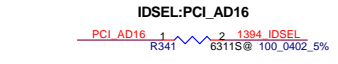


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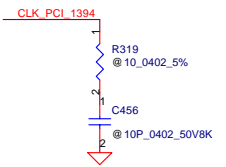
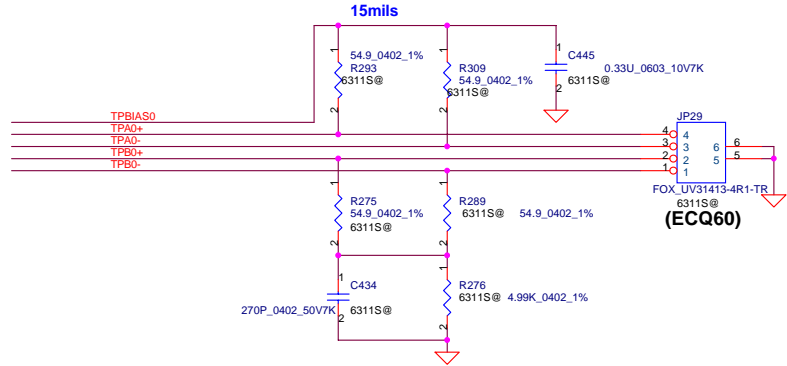
Compal Electronics, Inc.			
Title NEW CARD SOCKET			
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2005/10/20
2005/11/01
When use external EEPROM
Populate U14, R246, R253
Un-populate R261



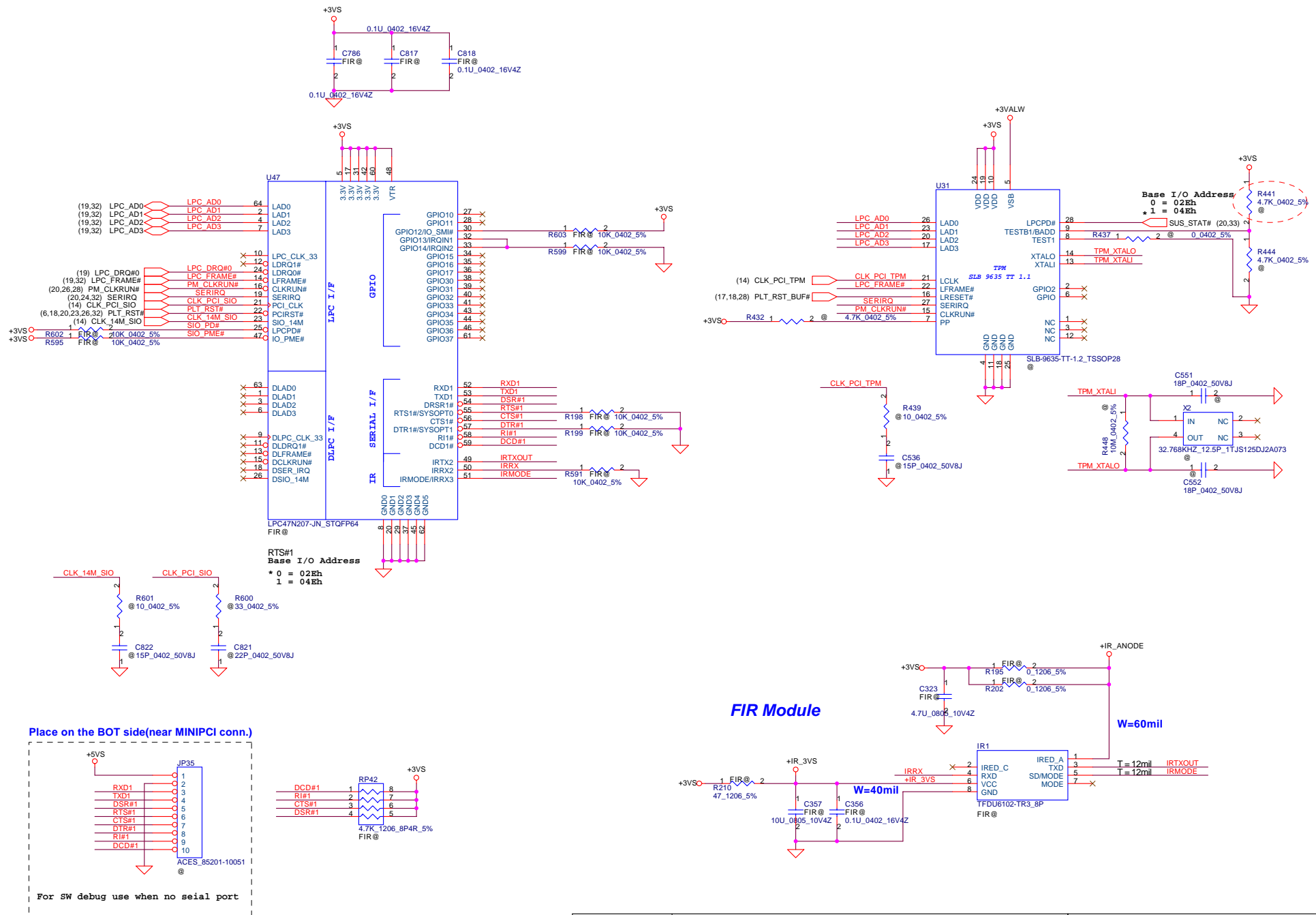
When use external BJT
Populate Q35, R279



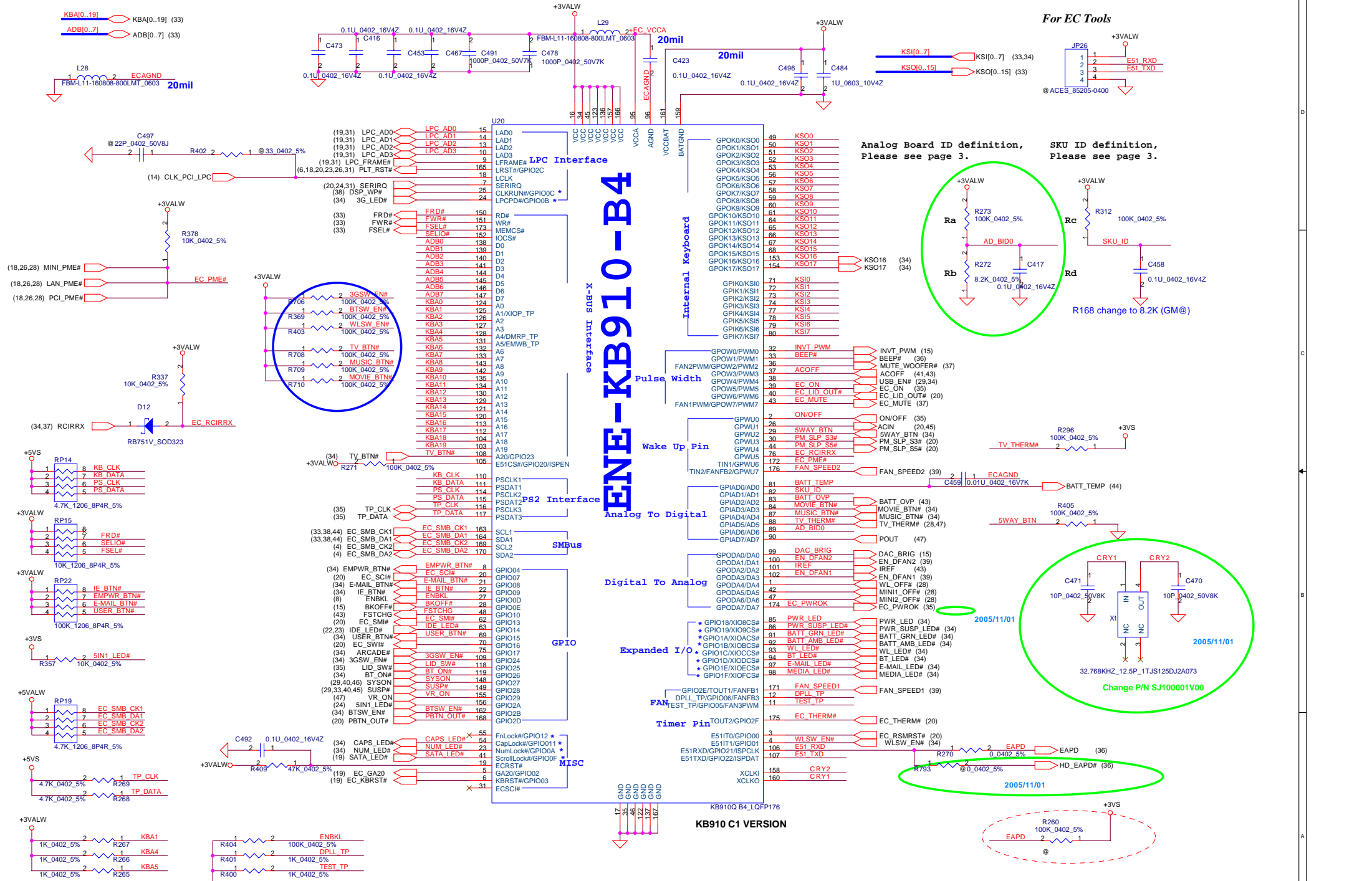
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		2006/06/20
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Compal Electronics, Inc.		
Title		
IEEE1394 VIA VT6311S		
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SUPER I/O SMsC LPC47N207



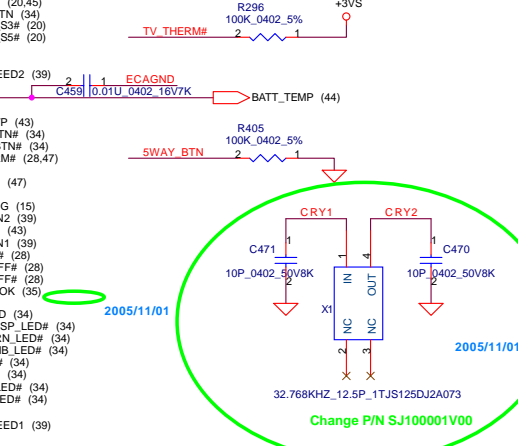
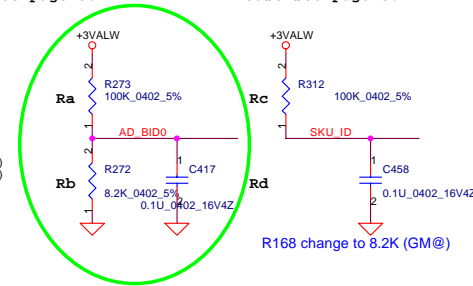
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For EC Tools

Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.



ENE-KB910-B4

Internal Keyboard

Pulse Width

Wake Up Pin

Analog To Digital

Digital To Analog

Expanded I/O

FAN

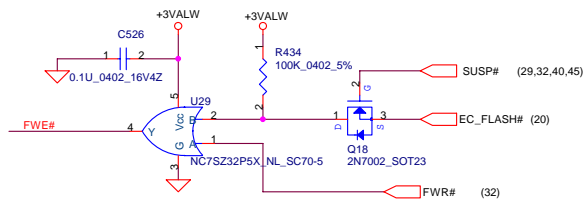
Timer Pin

MISC

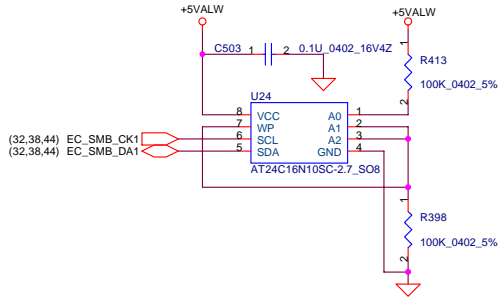
KB910 C1 VERSION

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		2006/06/20
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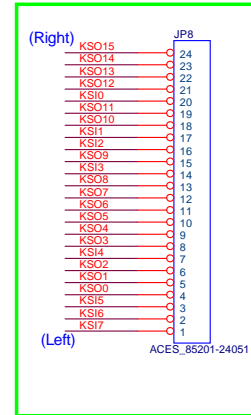
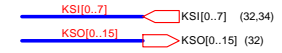
Compal Electronics, Inc.		
Title		
EC ENE KB910		
Size	Document Number	Rev
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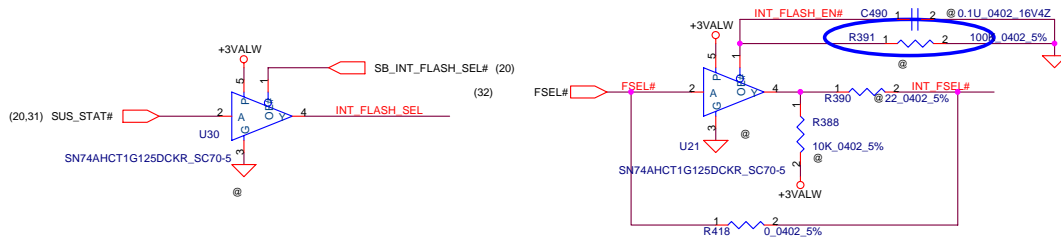
Check PCB Footprint



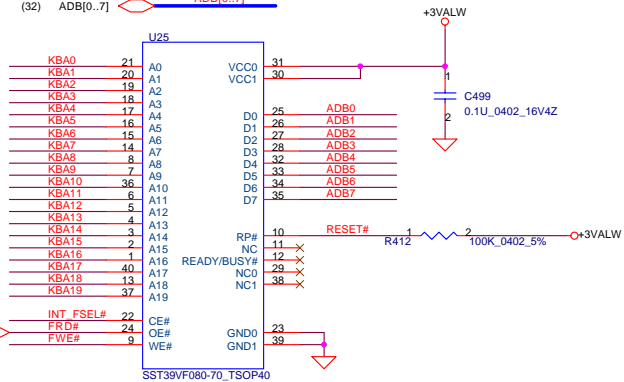
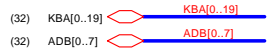
INT_KBD Conn.



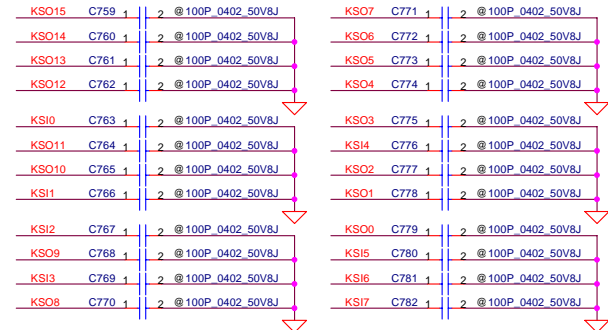
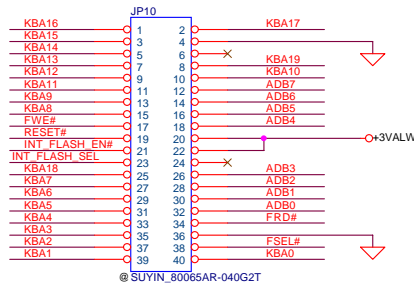
2005/11/03



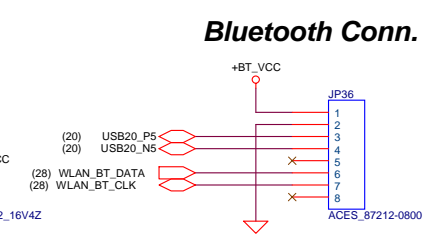
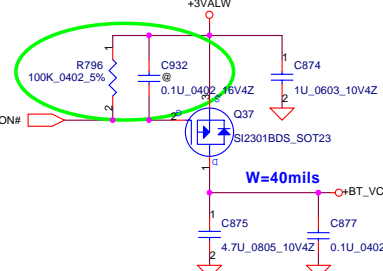
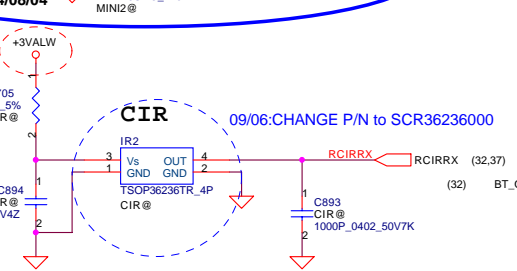
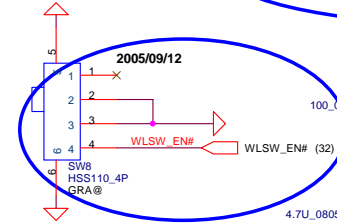
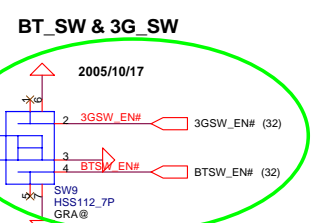
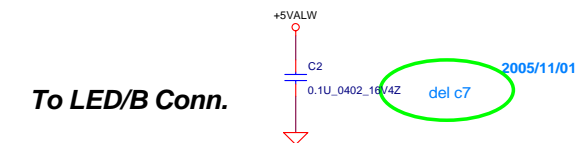
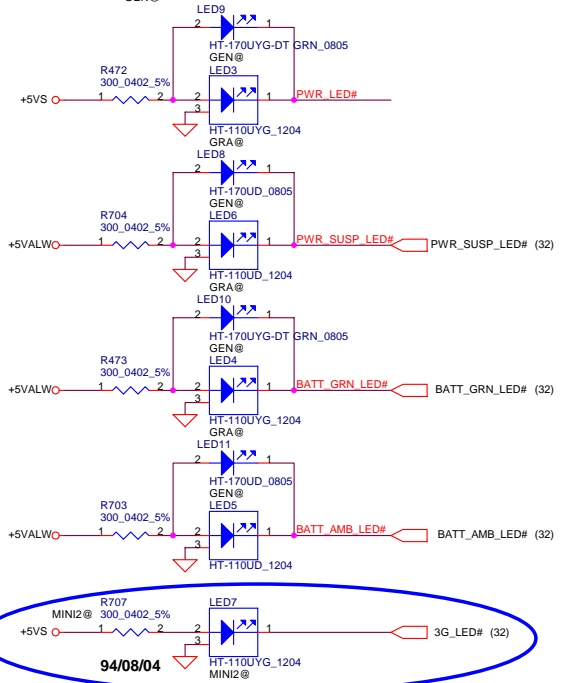
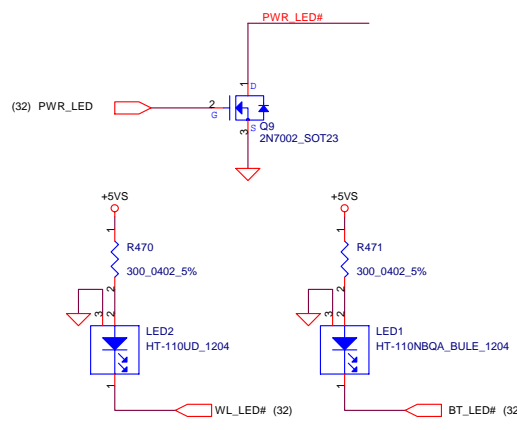
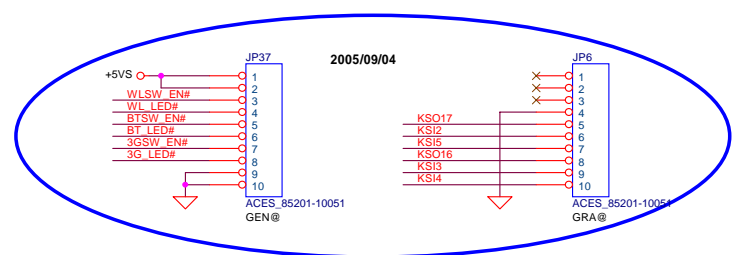
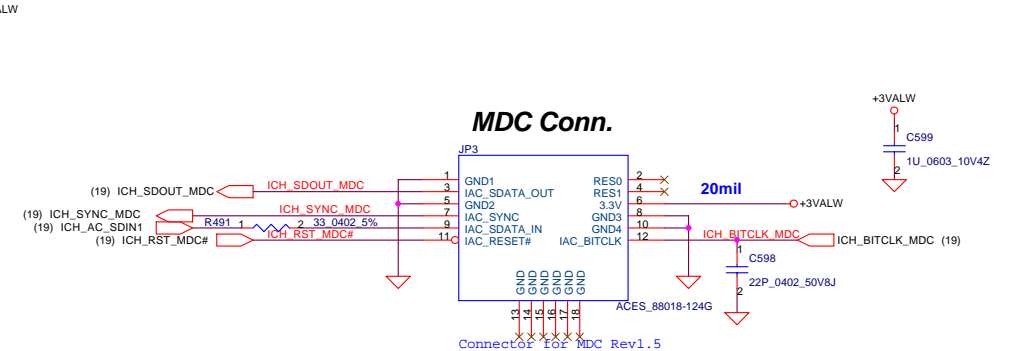
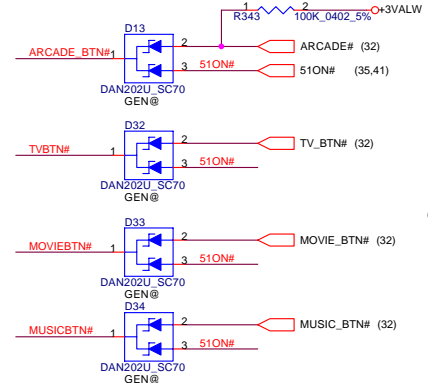
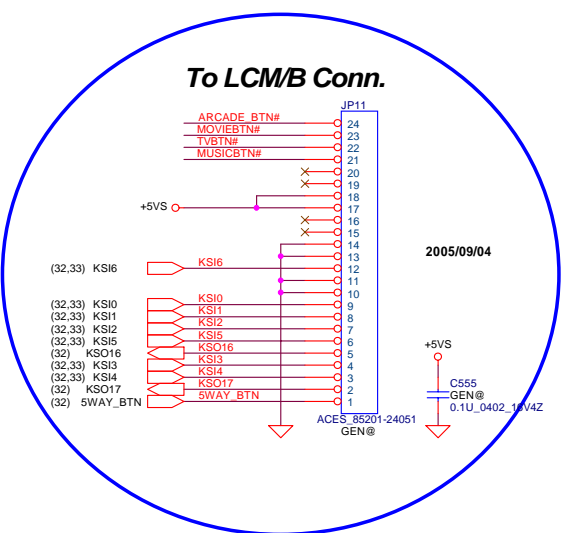
1MB Flash ROM



1MB ROM Socket



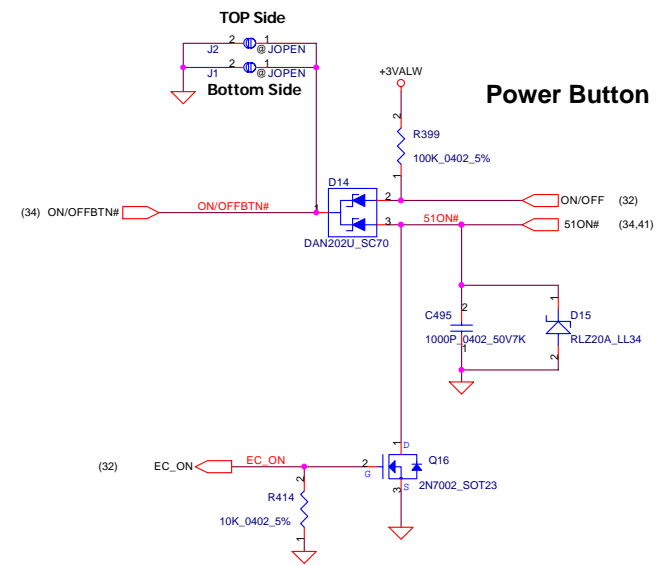
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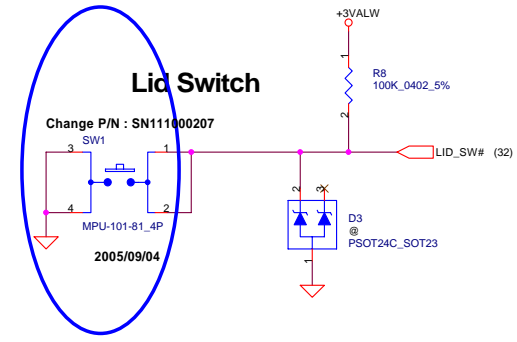
Geneva		Grapevine	
KSO16	KSO17	KSO16	KSO17
KSIO	VOL_UP		
KSII	RIGHT		
KSII	PLAY	PLAY	
KSII	STOP	STOP	VOL_UP
KSII	NEXT	NEXT	VOL_DOWN
KSII	REV	REV	ARCADE_TV
KSII			RECORD

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

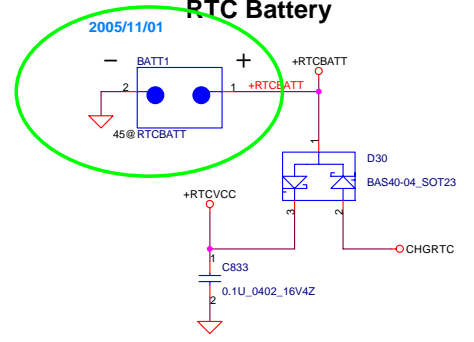
ON/OFF switch



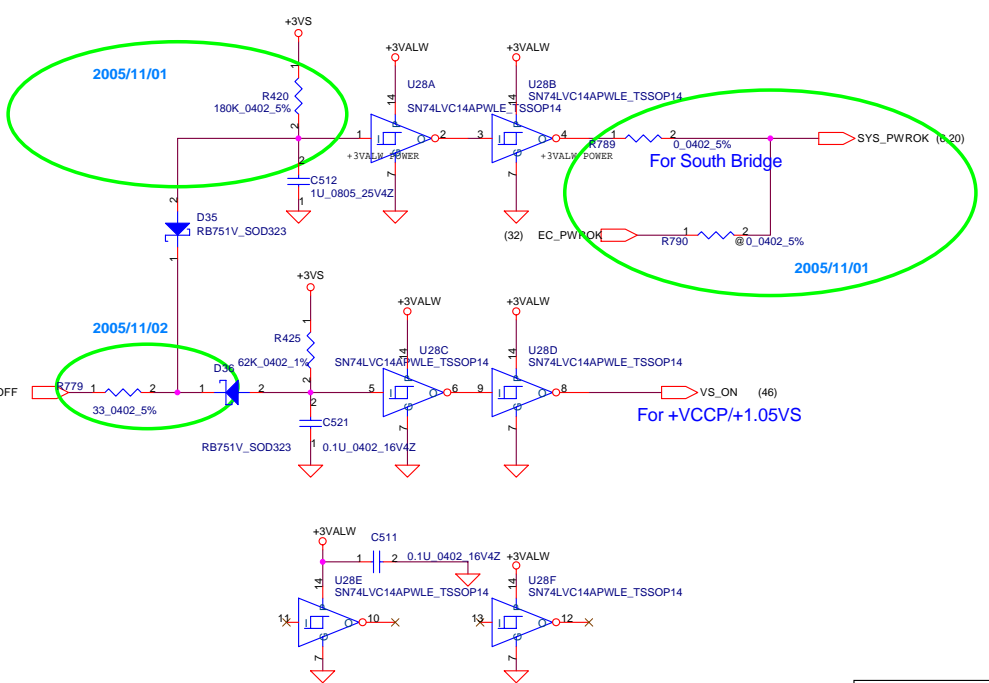
Lid Switch



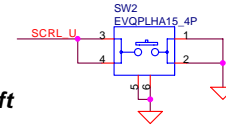
RTC Battery



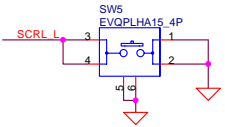
Power ON Circuit



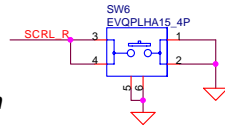
Scroll Up



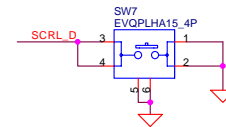
Scroll Left



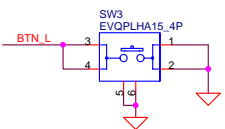
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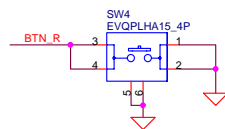
Scroll Down



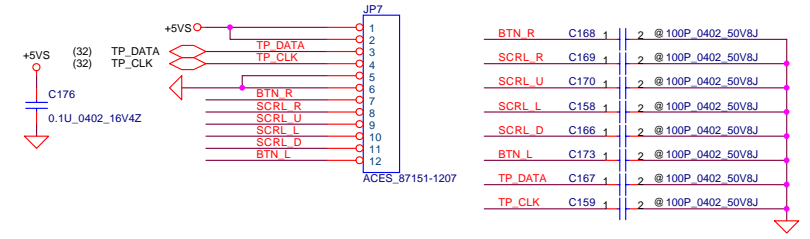
Left



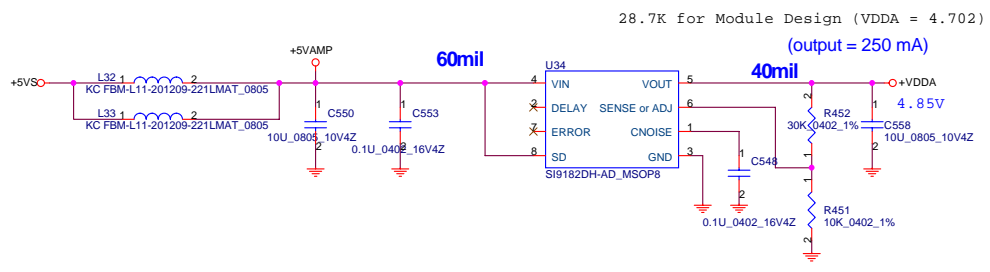
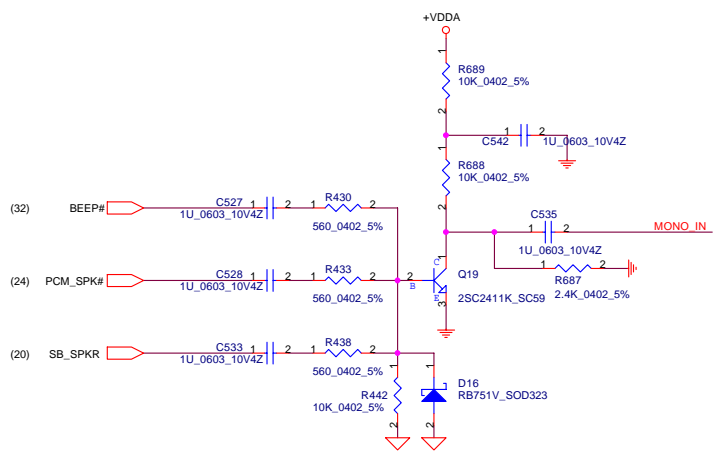
Right



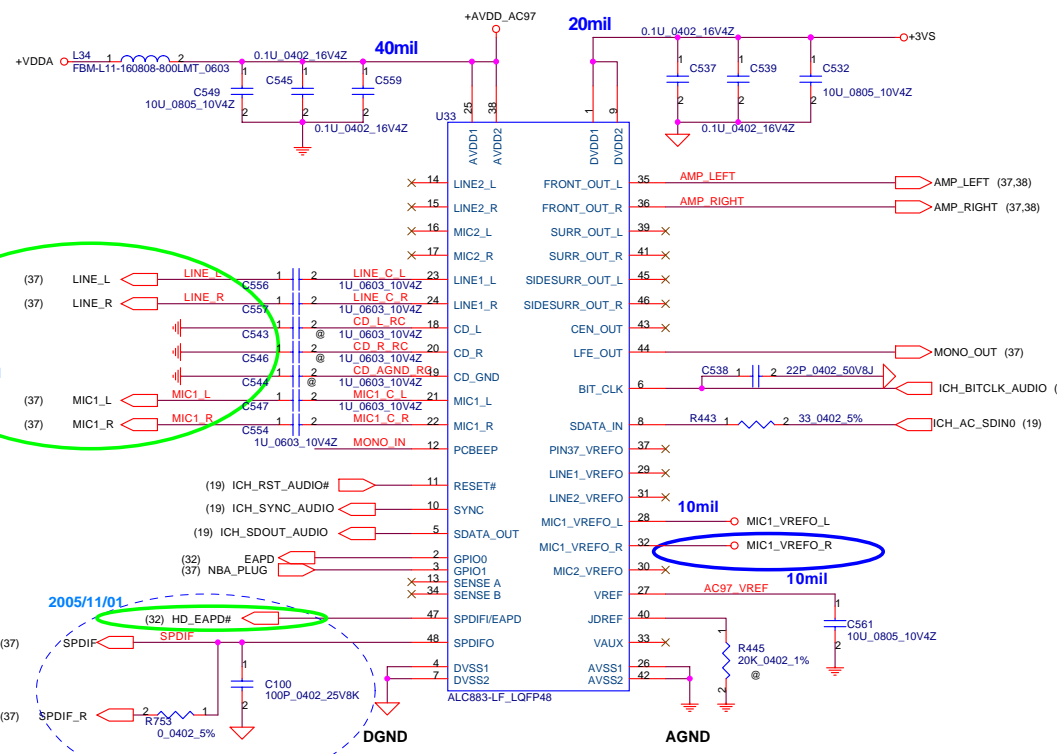
To TP/B Conn.



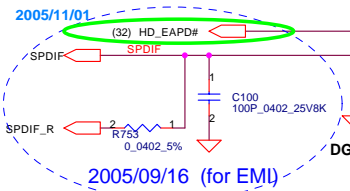
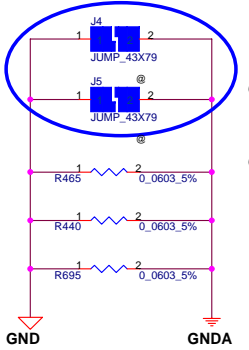
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Power OK, Reset and RTC Circuit, TP	
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		HBL51 LA-3081P		Date: Wednesday, November 09, 2005	
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HD Audio Codec



2005/11/01



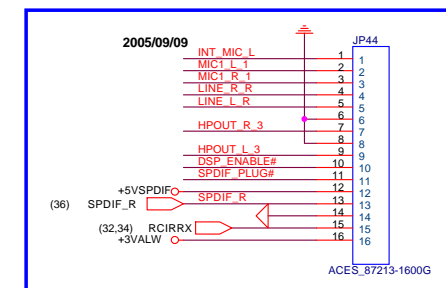
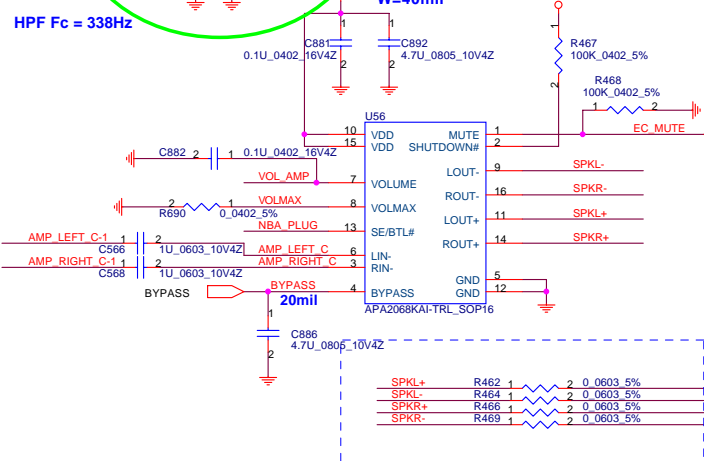
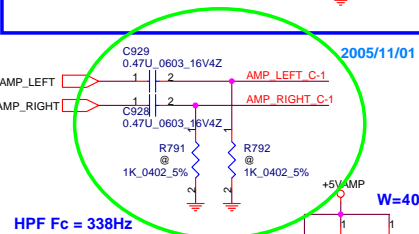
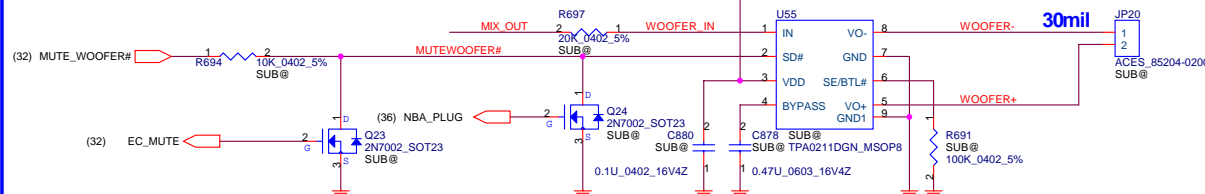
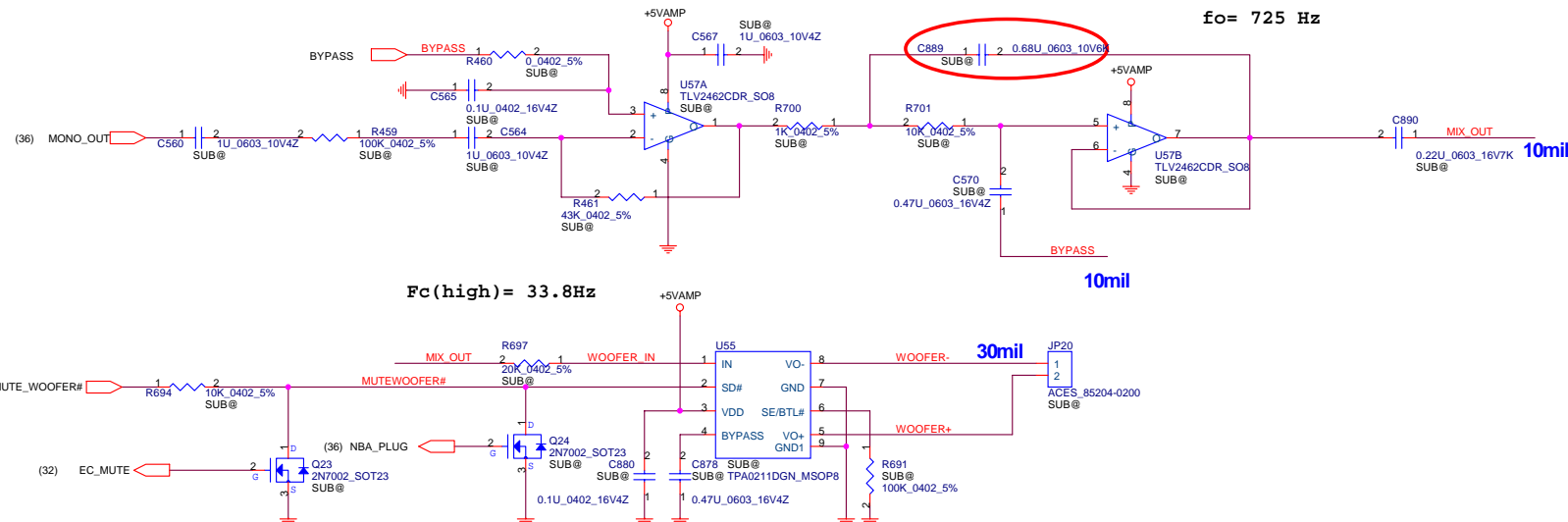
2005/09/16 (for EMI)

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				HD Audio Codec ALC883	
Size B	Document Number			Rev	0.2
				HBL51 LA-3081P	
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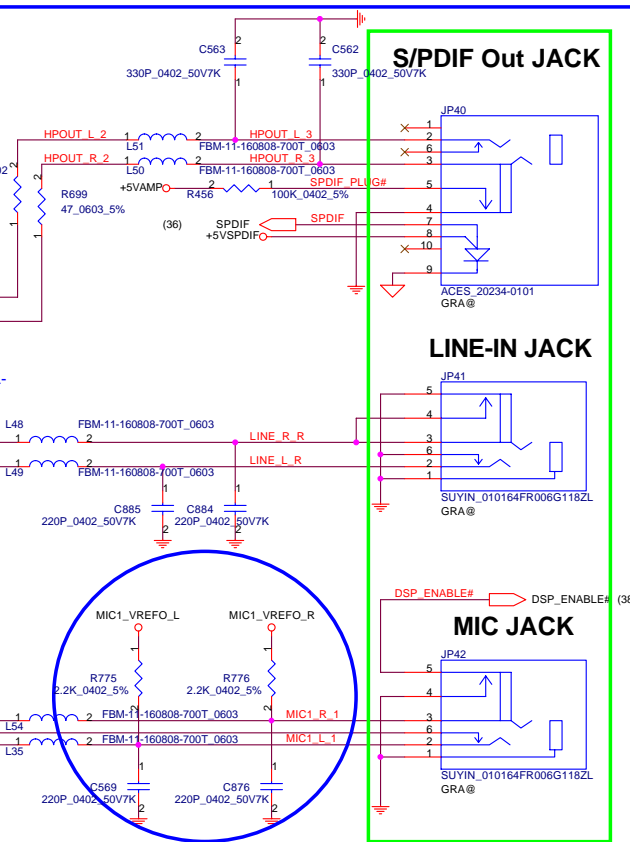
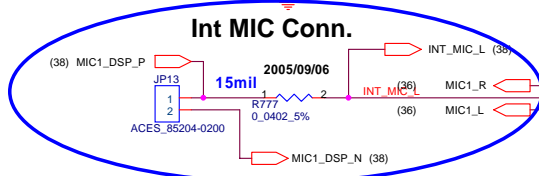
Subwoofer

fo = 725 Hz

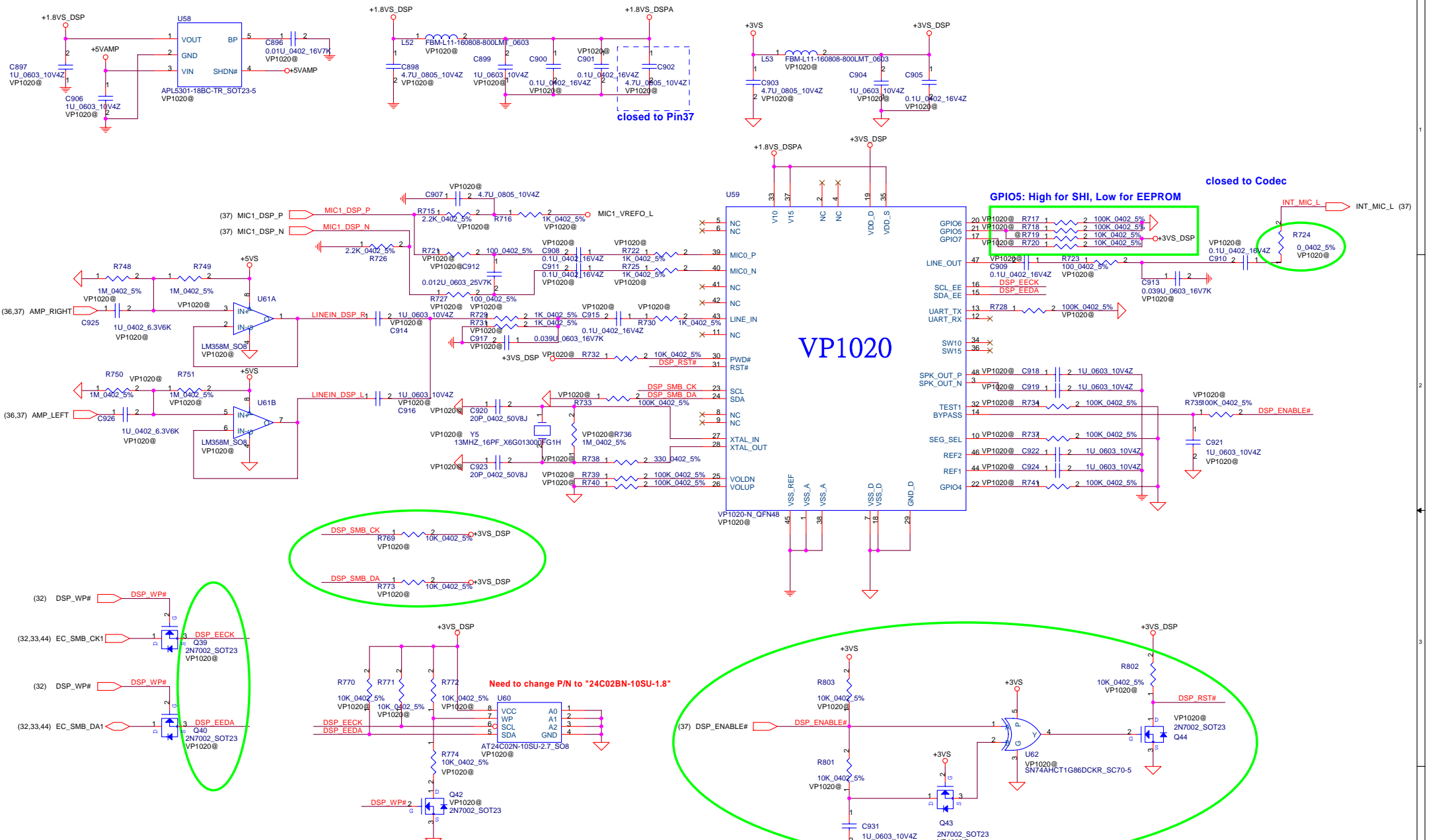
Fc(high) = 33.8Hz



20mil Speaker Conn.



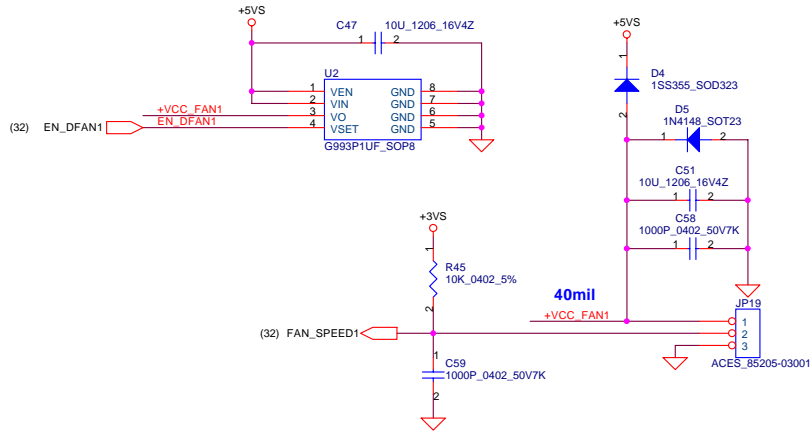
Security Classification		Compal Secret Data		Title		
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Amplifier & Audio Jack & Subwoofer		
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				Date:	Wednesday, November 09, 2005	Sheet 37 of 47



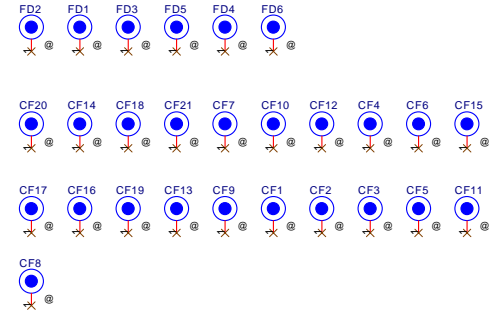
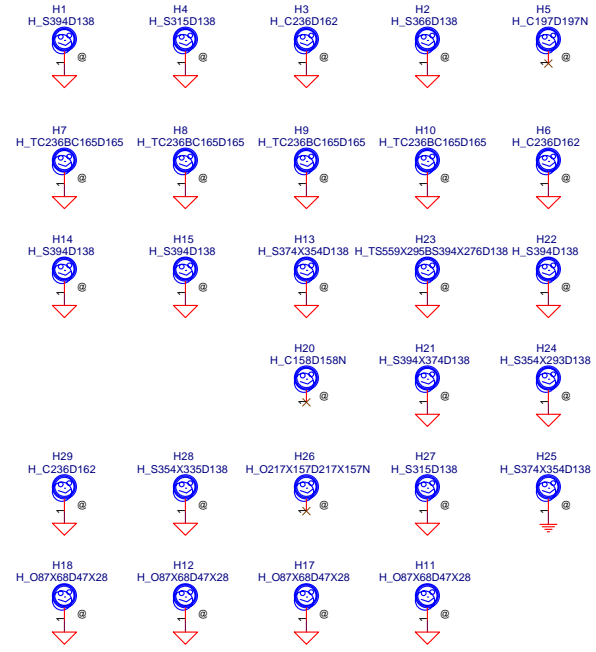
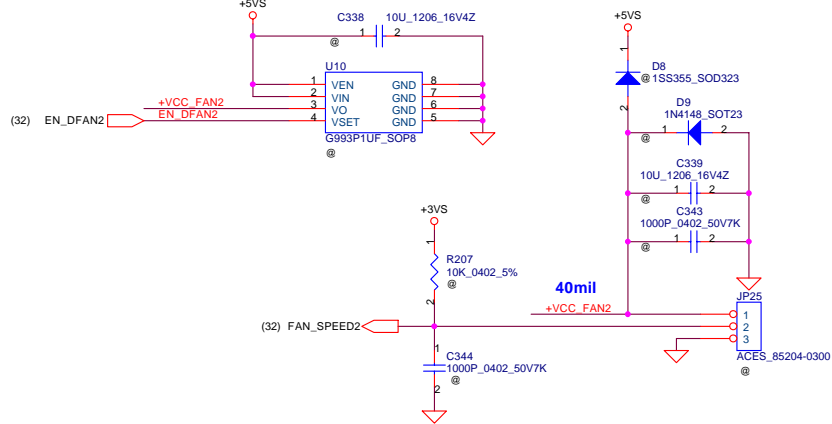
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Title DSP			
Size	Document Number	Rev	
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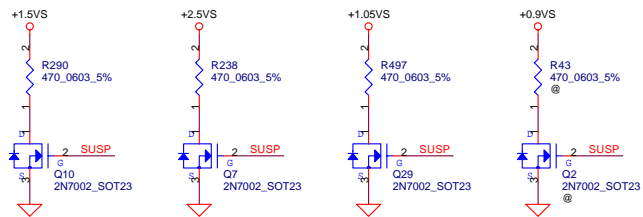
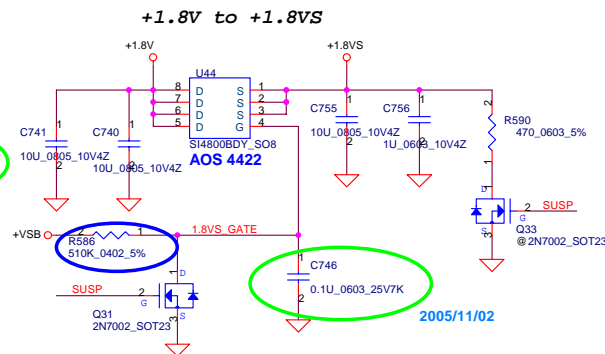
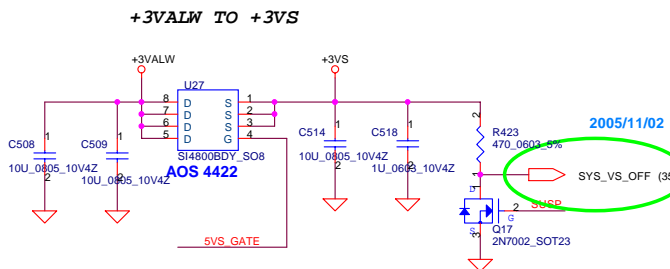
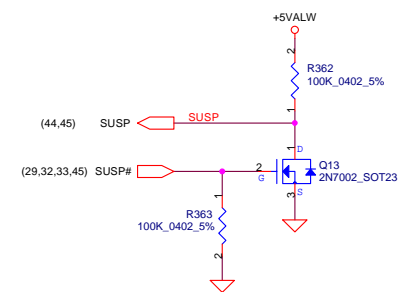
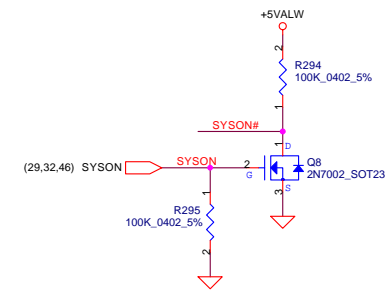
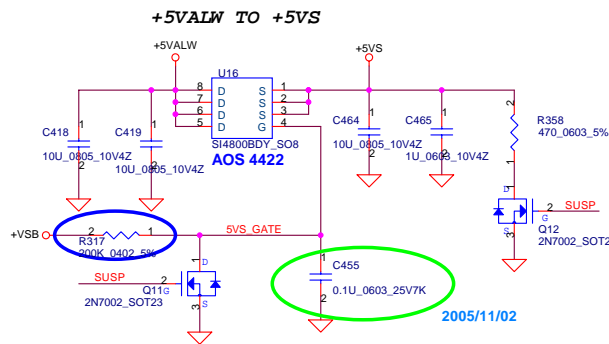
FAN1 Conn



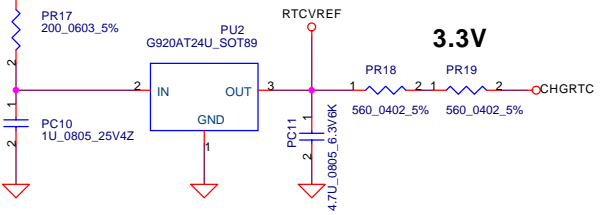
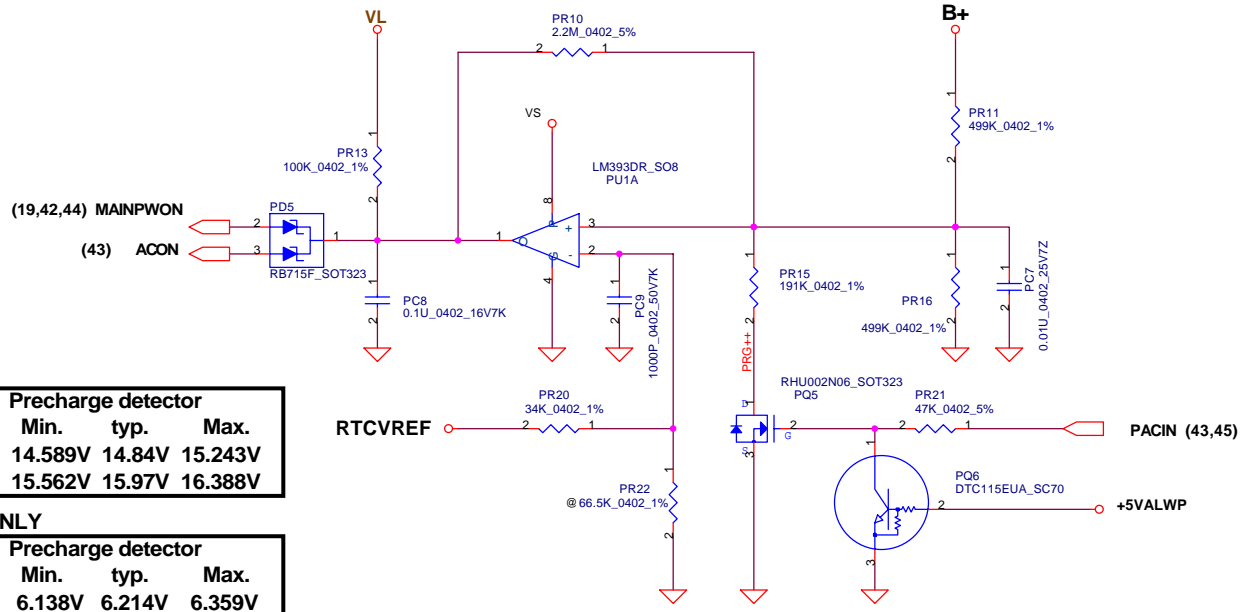
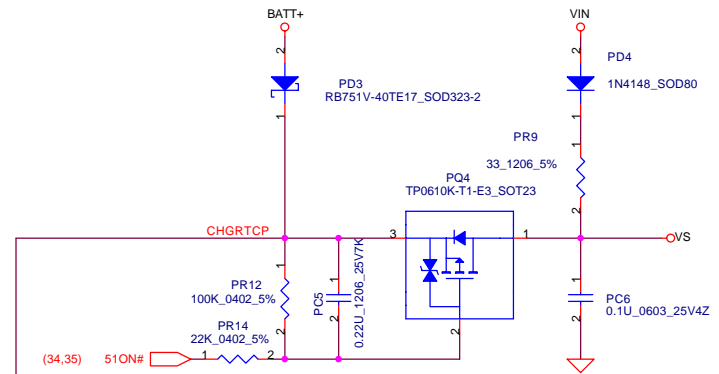
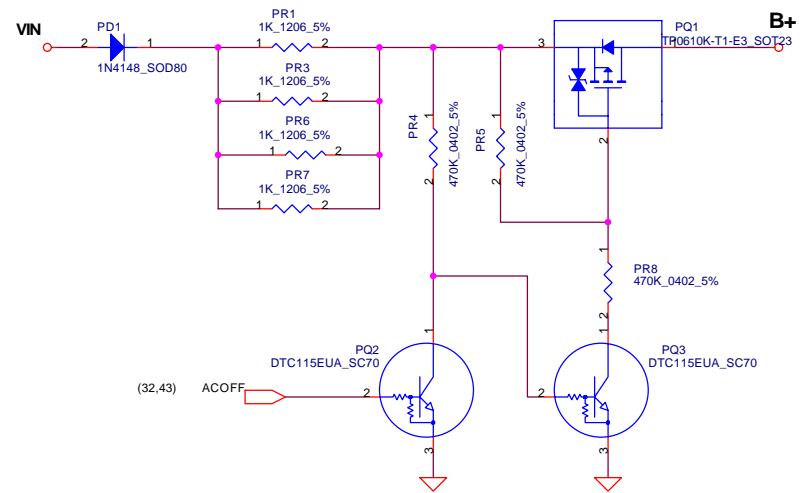
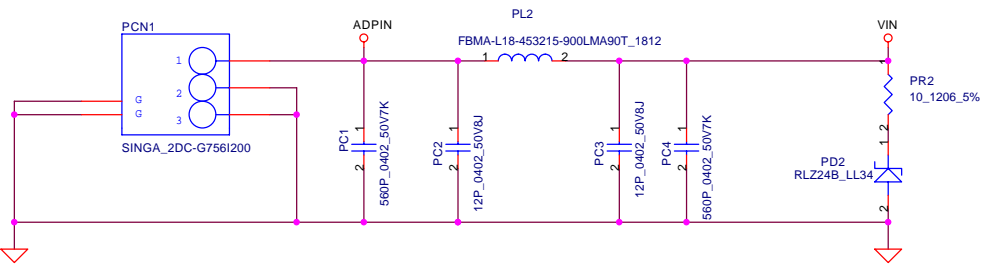
FAN2 Conn



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Size	Document Number	Rev		
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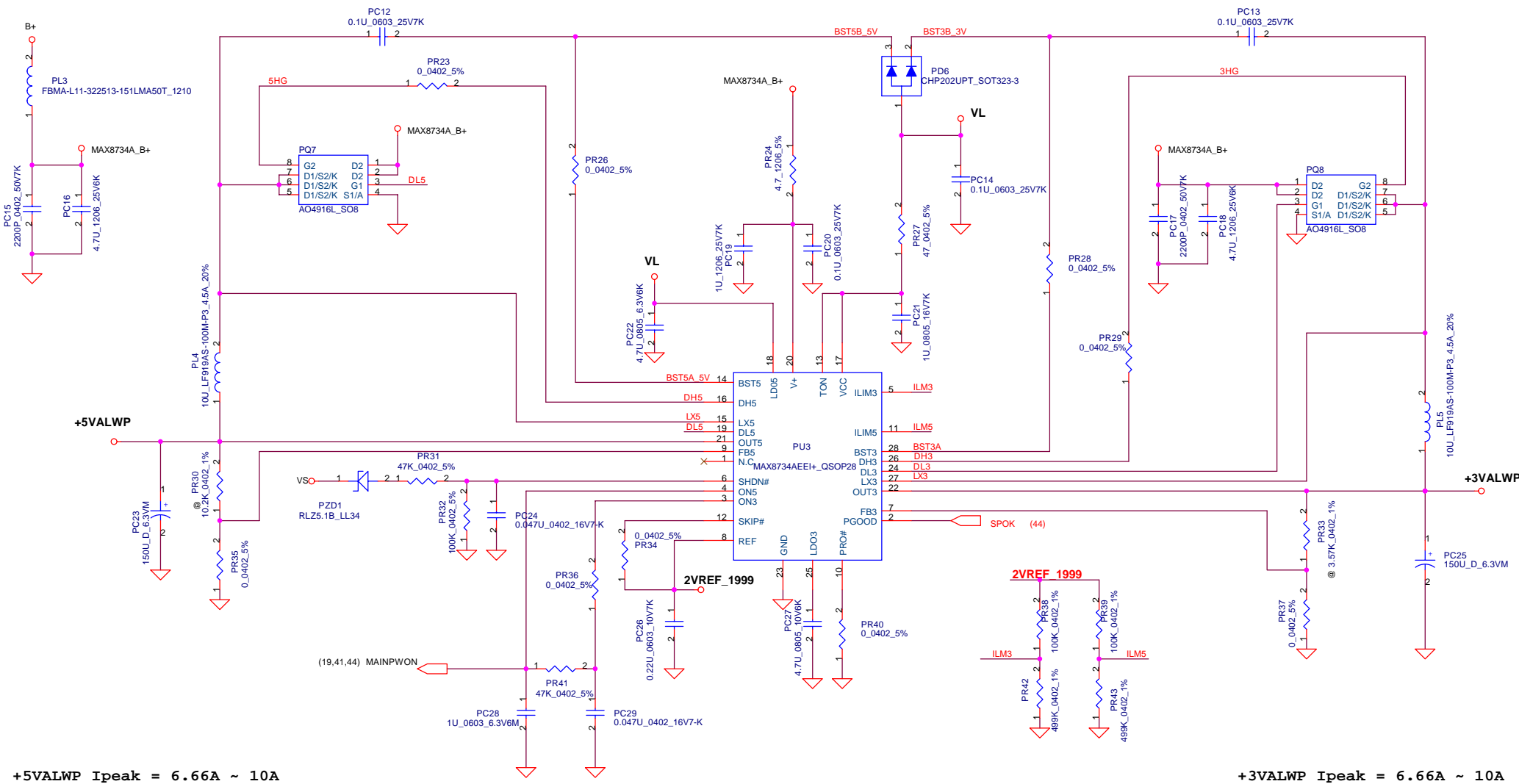
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ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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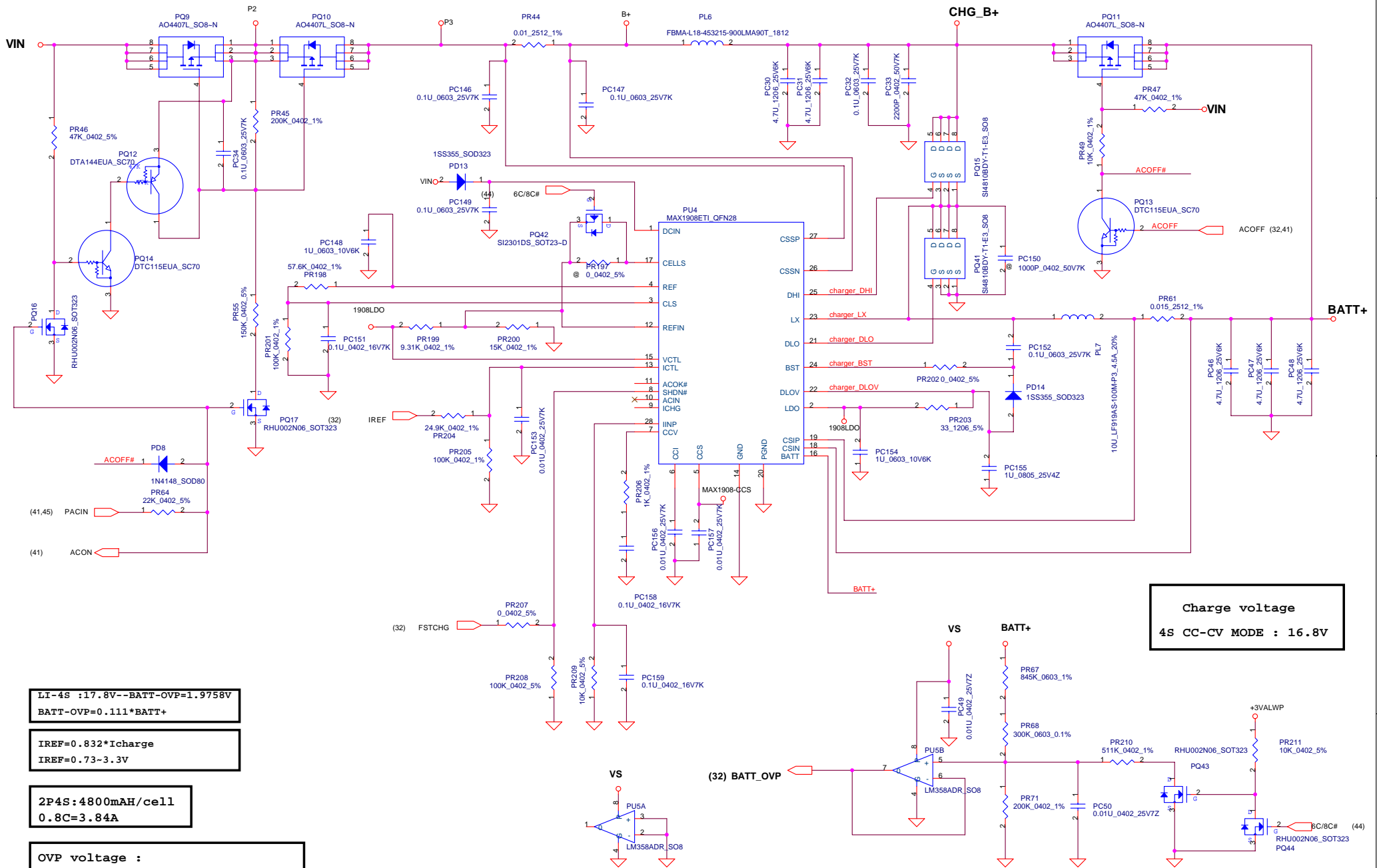


+5VALWP Ipeak = 6.66A ~ 10A

+3VALWP Ipeak = 6.66A ~ 10A

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I_{adp}=0~4.74A(90W)



Charge voltage
4S CC-CV MODE : 16.8V

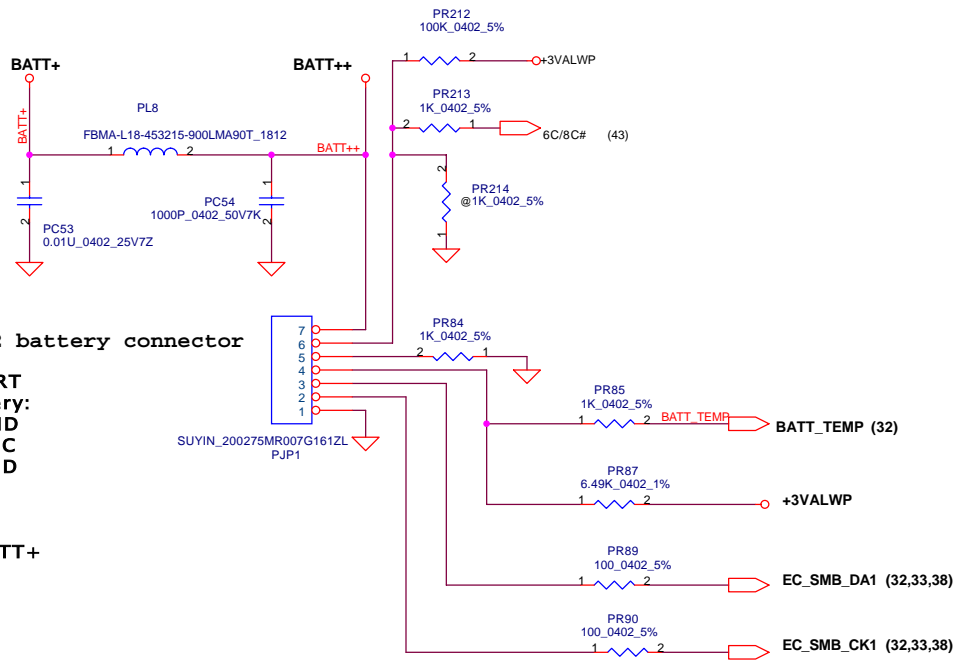
LI-4S : 17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

2P4S:4800mAh/cell
0.8C=3.84A

OVP voltage :
LI-3S : 17.8V---BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

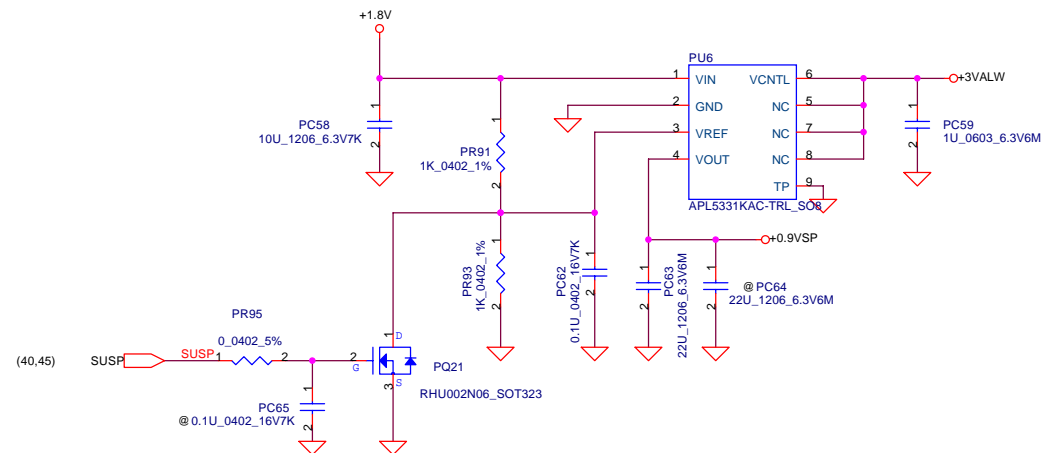
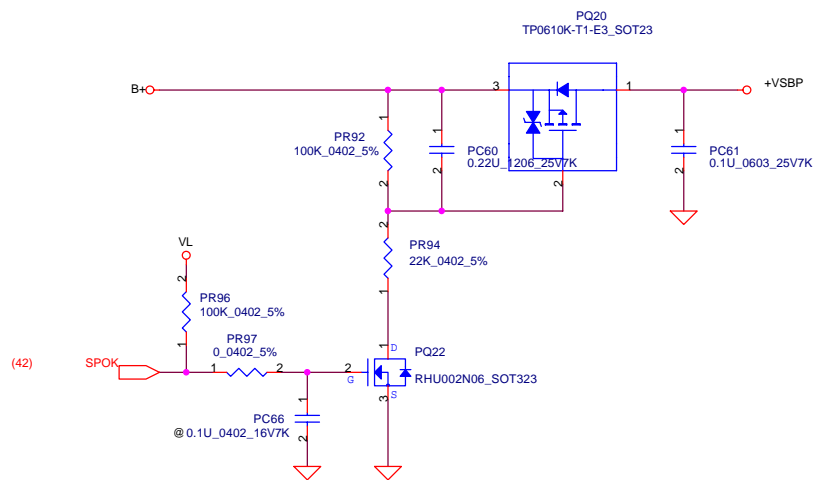
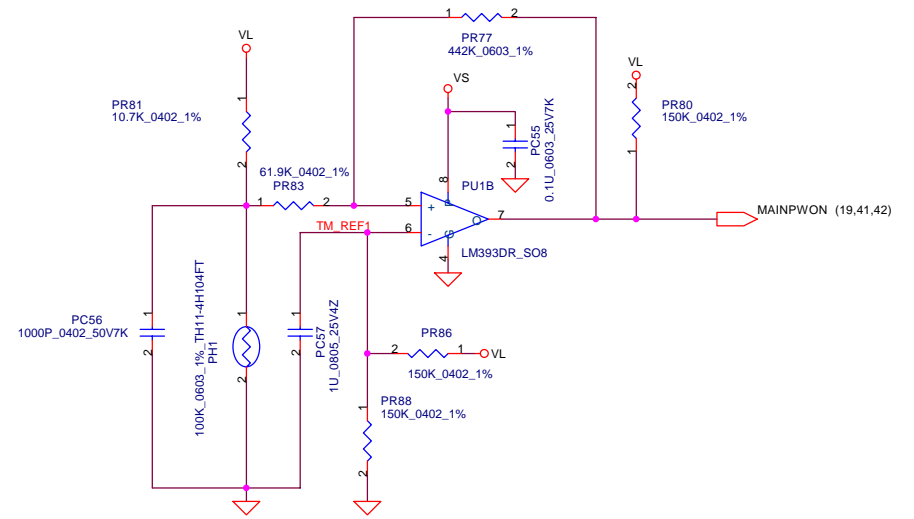
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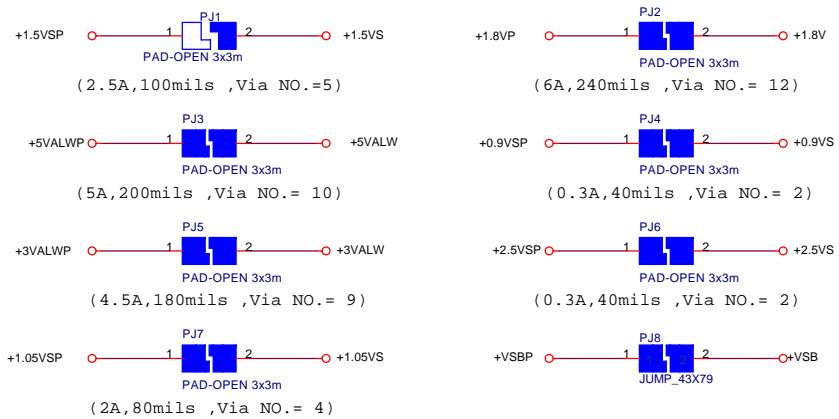
PJP2 battery connector

SMART Battery:
 1.GND
 2.SMC
 3.SMD
 4.TS
 5.B/I
 6.ID
 7.BATT+

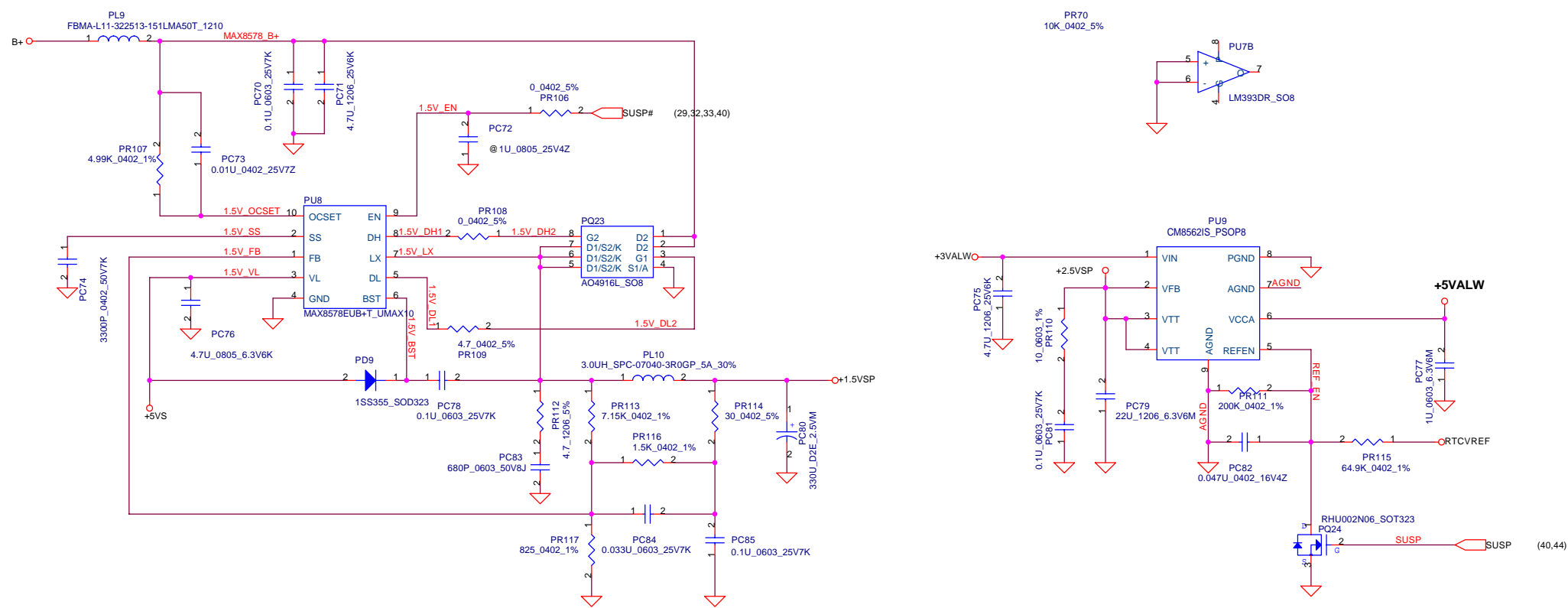
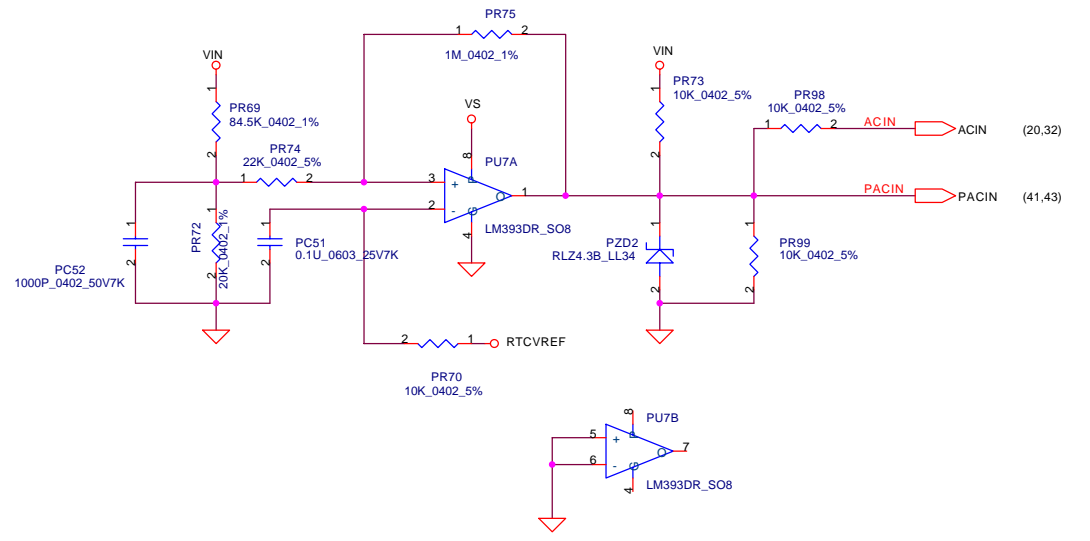
PH1 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C



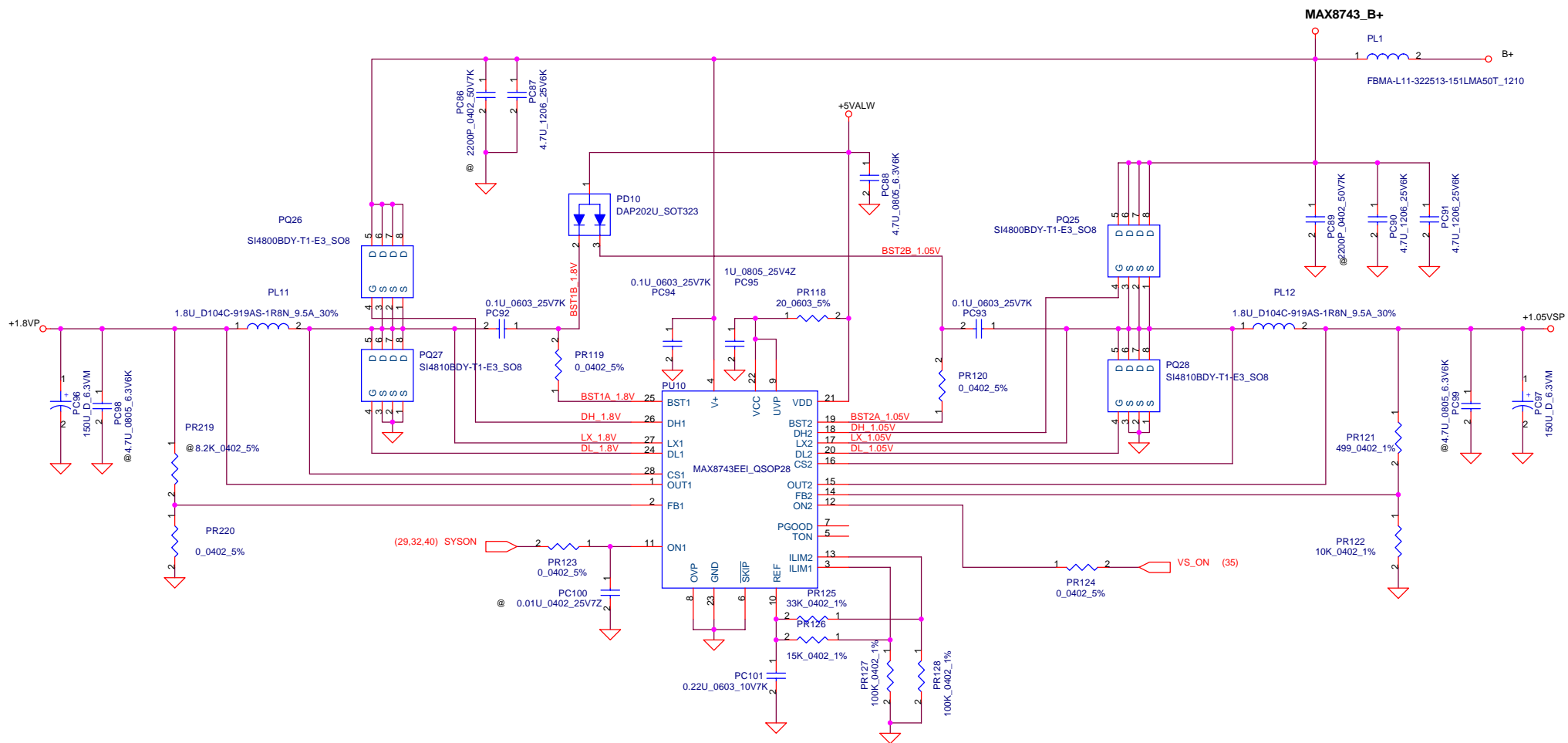
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Vin Detector
17.90V/17.24V

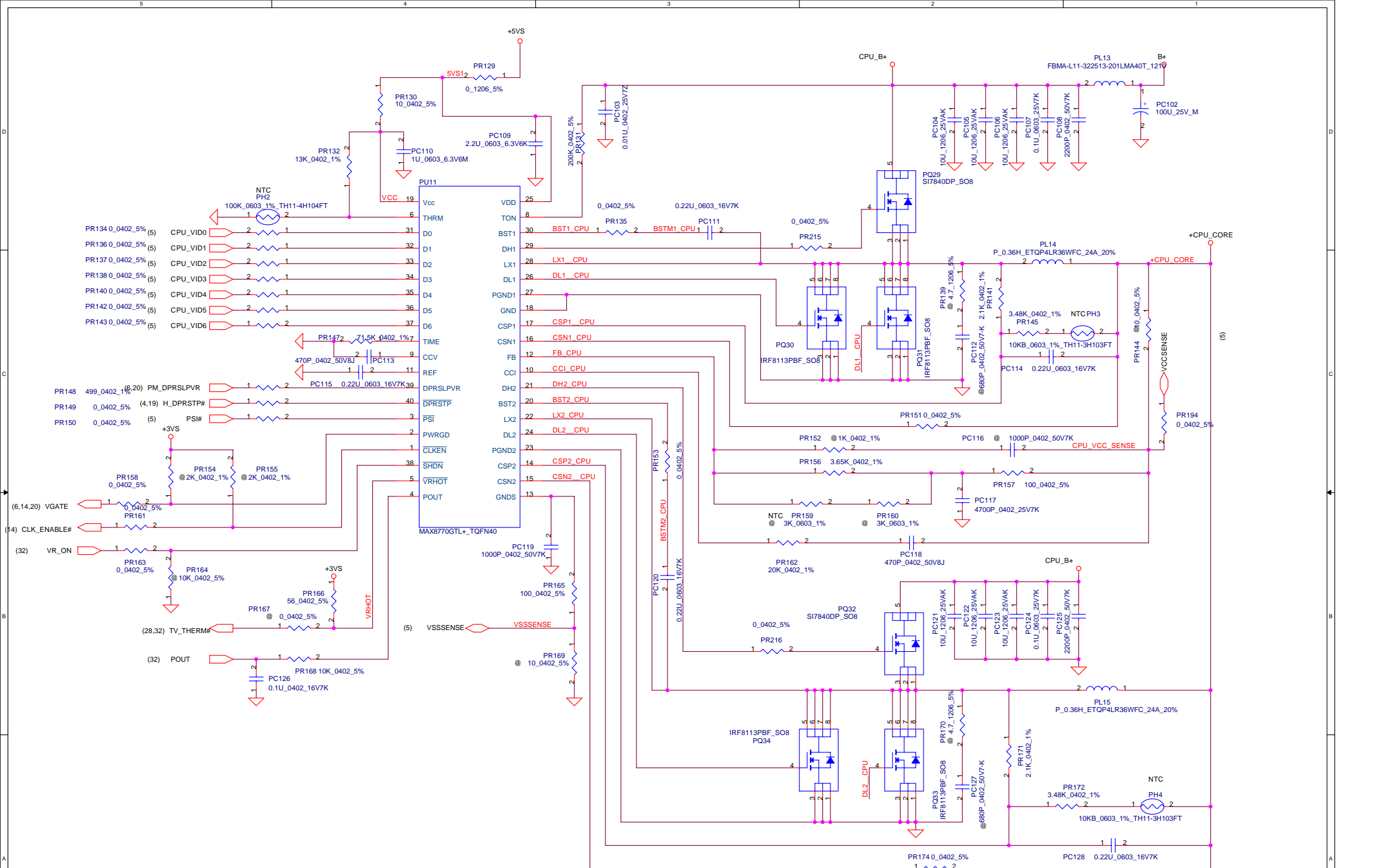


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Compal Electronics, Inc.		
Title		
+1.05VSP/+1.8VSP		
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